EE 505

Lecture 19

ADC Design

- The Flash ADC
- Comparators

Review from Last Lecture

Relative Statistical Characterization of R-based DACs

Resolution = 10

$A_{\rho R}$ = 0.02µm

R_{nom} = 1000

Total Area 2048 μm^2

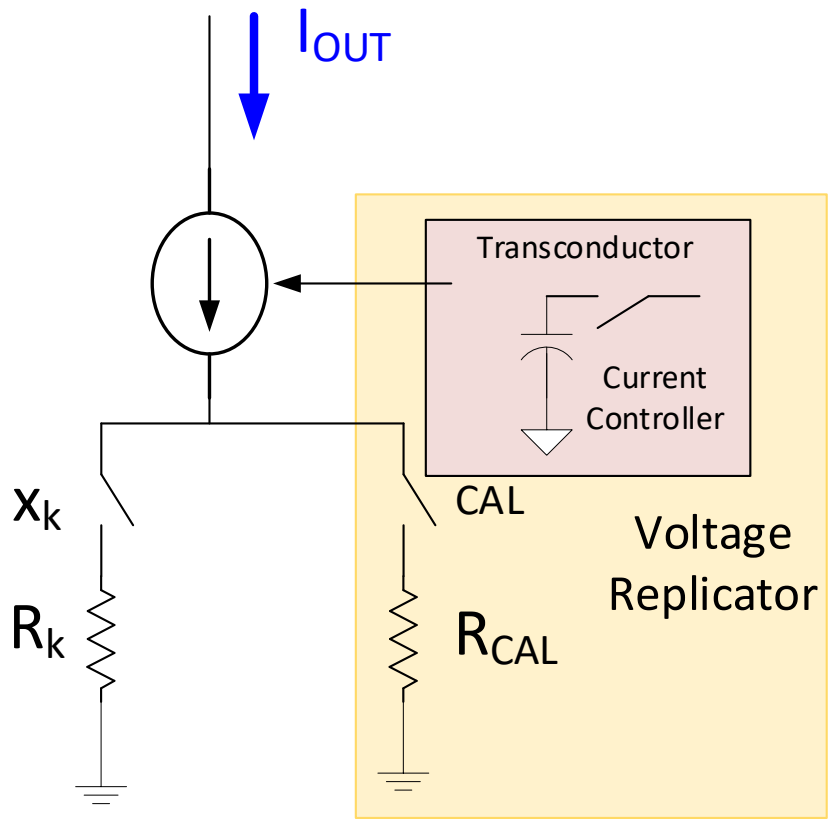
Resistor Sigma= 14.1421

INL_{target} = 0.5 LSB

Yield =28.5%

Architecture	INL(LSB)		DNL(LSB)		INL Yield
	Mean	Sigma	Mean	Sigma	
String	0.385	0.118	0.049	0.0047	84.0
Binary Weighted	0.367	0.128	0.470	0.228	84.9
R-2R Series	0.609	0.295	1.021	0.610	41.4
R-2R Parallel	0.737	0.357	1.225	0.732	28.5
Slice Scaled (1.7) Series R-2R	0.399	0.153	0.556	0.286	76.4

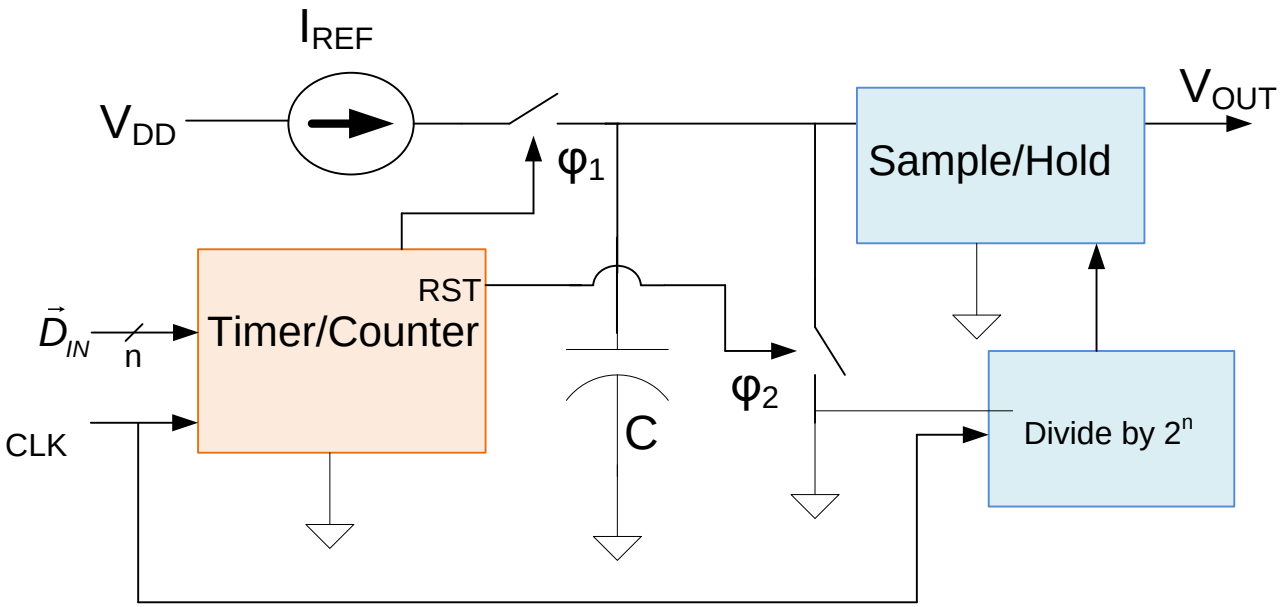
Floating Current Copier



Review from Last Lecture

DAC Architectures

Single Slope

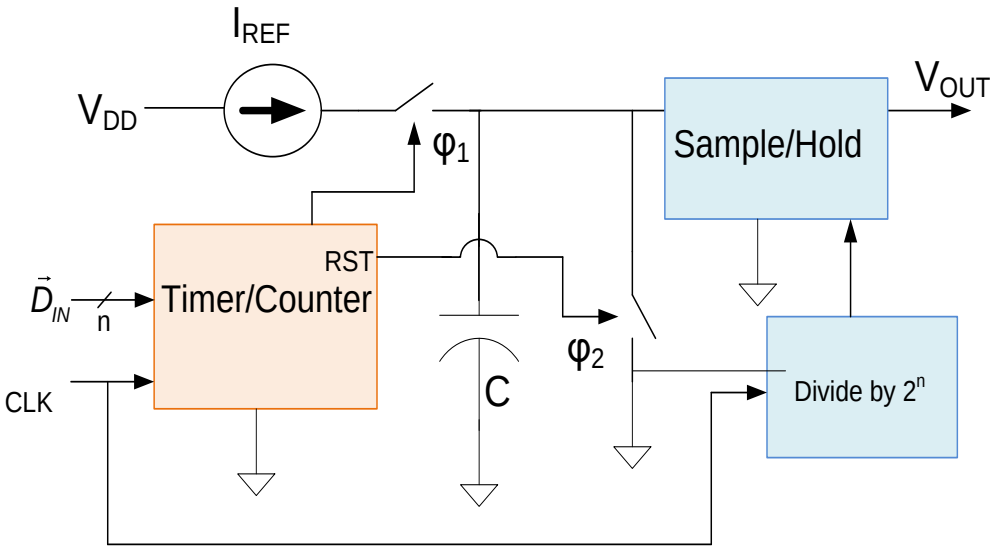


Single-Slope DAC

Review from Last Lecture

DAC Architectures

Single Slope



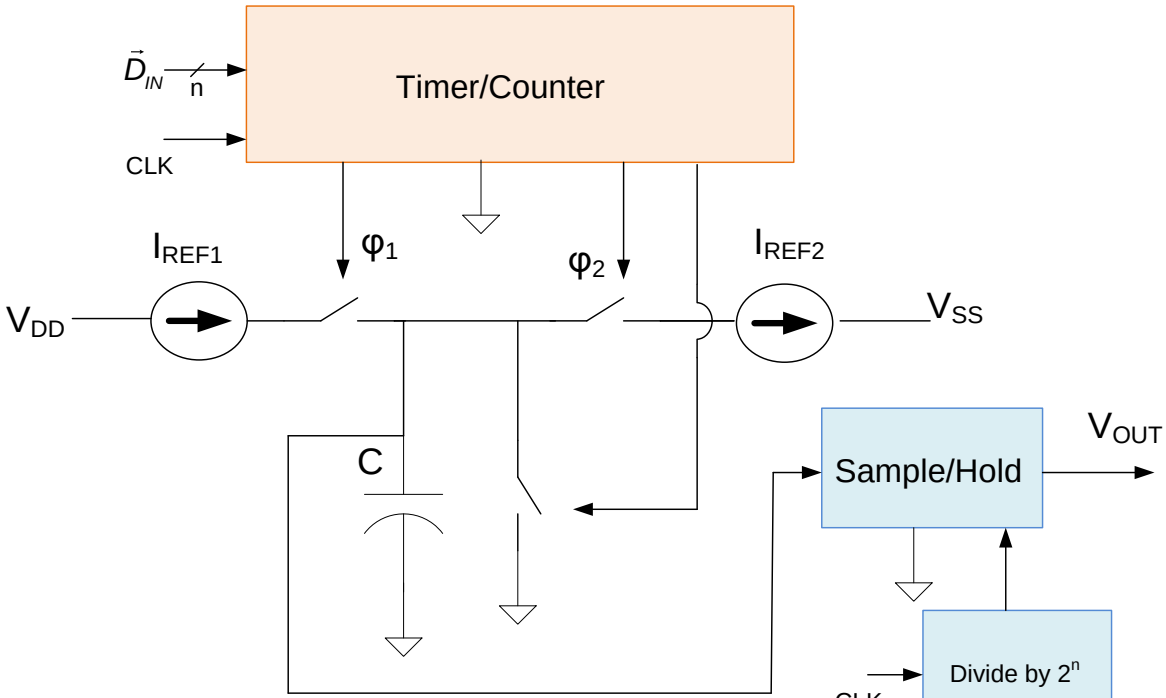
Single-Slope DAC

Segmentation can be used to increase speed ($I_{REF1}=I_{REF}/2\text{^}n_1$)

Review from Last Lecture

DAC Architectures

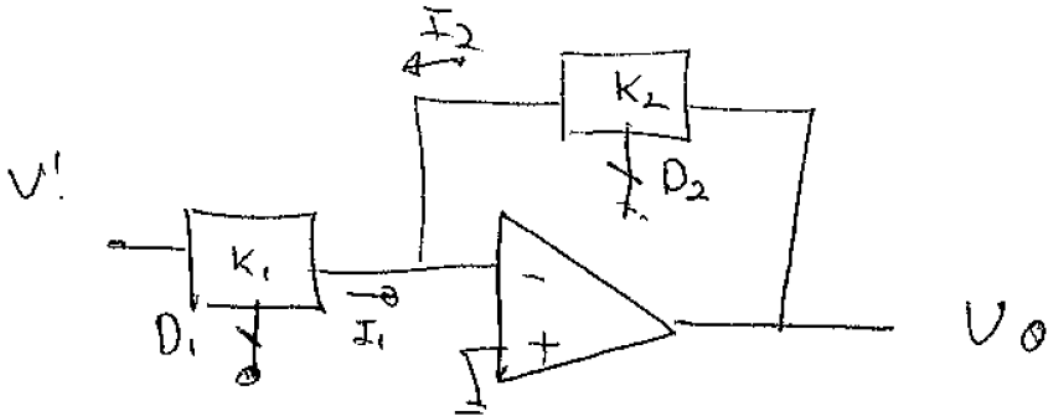
Dual Slope



Dual-Slope DAC

Review from Last Lecture

Multiplying and Dividing DACs



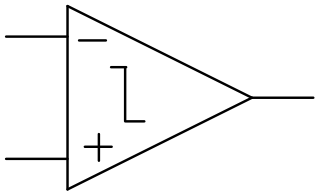
$$\begin{cases} I_1 = K_1 V_i D_1 \\ I_2 = V_o D_2 K_2 \end{cases}$$

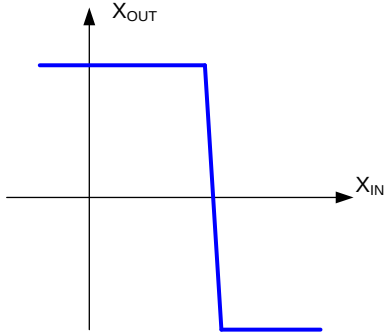
$$\therefore \quad V_o = \frac{D_1}{D_2}\left[\frac{-K_1}{K_2} V_i\right]$$

Can create various nonlinear relationships with MDACs and Op Amps

Analog to Digital Converters

The conversion from analog to digital in ALL ADCs is done with comparators

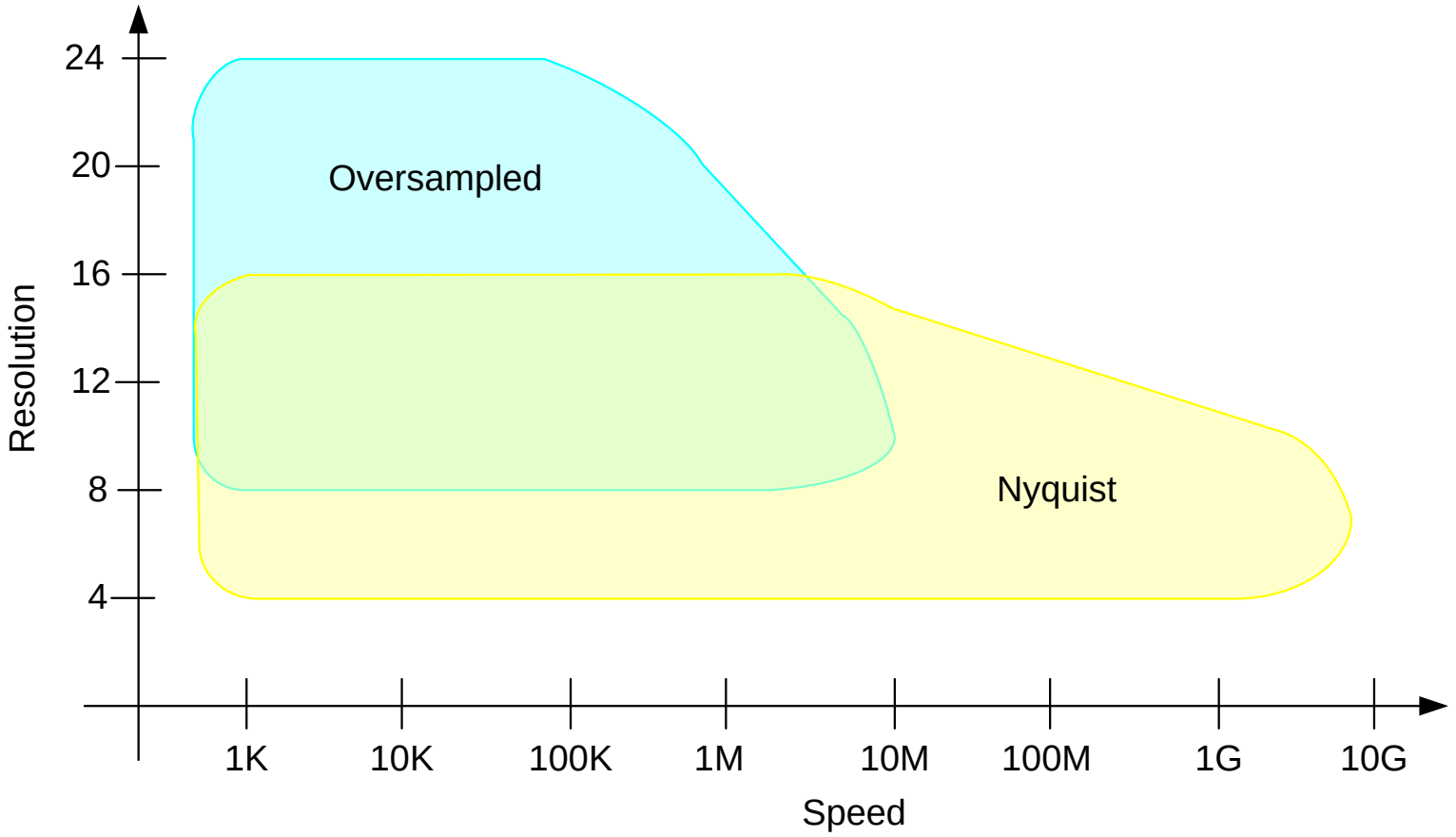




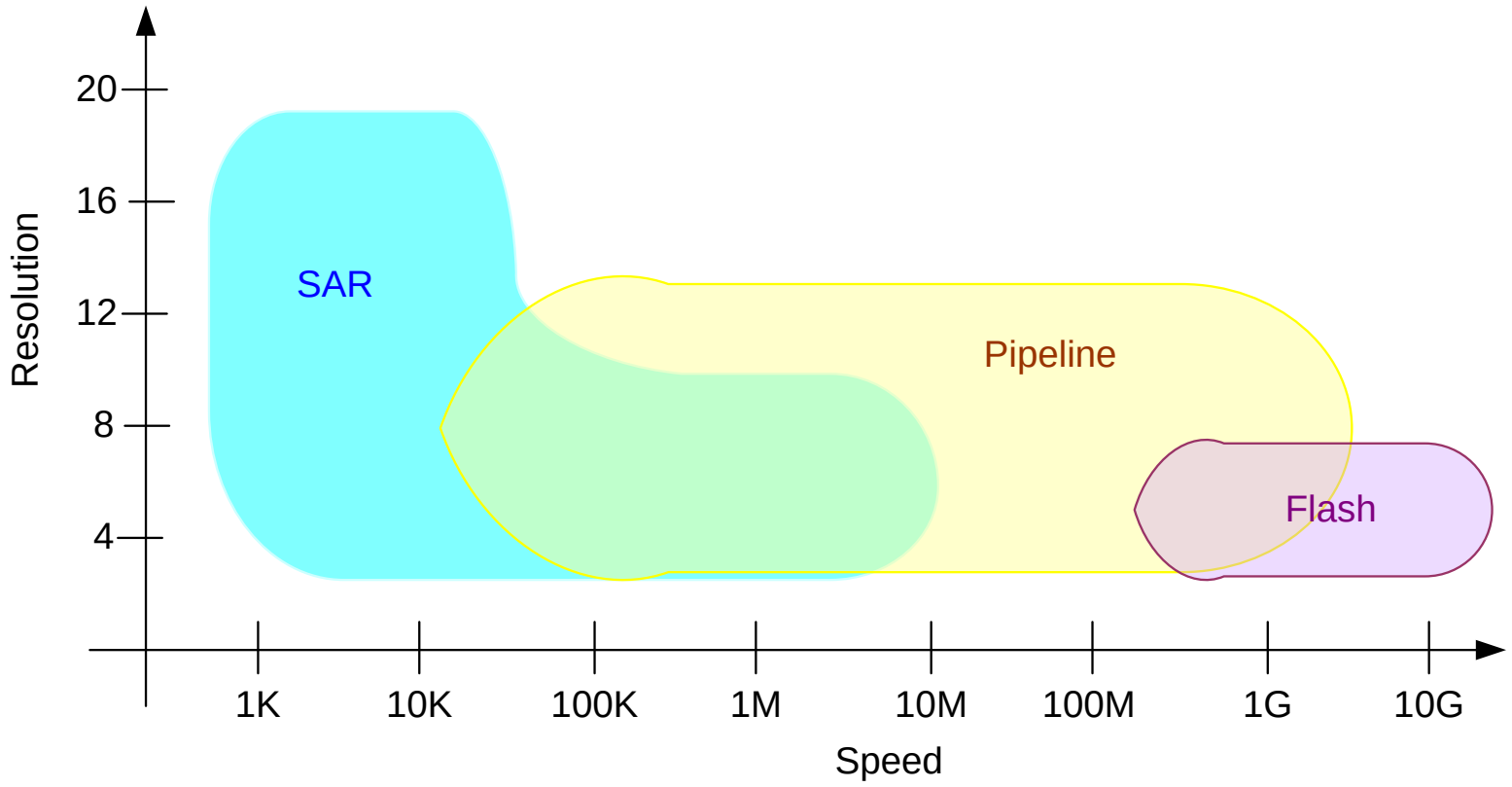
ADC design is primarily involved with designing comparators and embedding these into circuits that are robust to nonideal effects

Review from Last Lecture

Data Converter Type Chart



Nyqyist Rate Usage Structures



Flash is the least used as a stand-alone structure but widely used as a subcomponent in SAR and Pipelined Structures

Review from Last Lecture

ADC Types

Nyquist Rate

- Flash
- Pipeline
- Two-Step Flash
- Multi-Step Flash
- Cyclic (algorithmic)
- Successive Approximation
- Folded
- Dual Slope

Over-Sampled

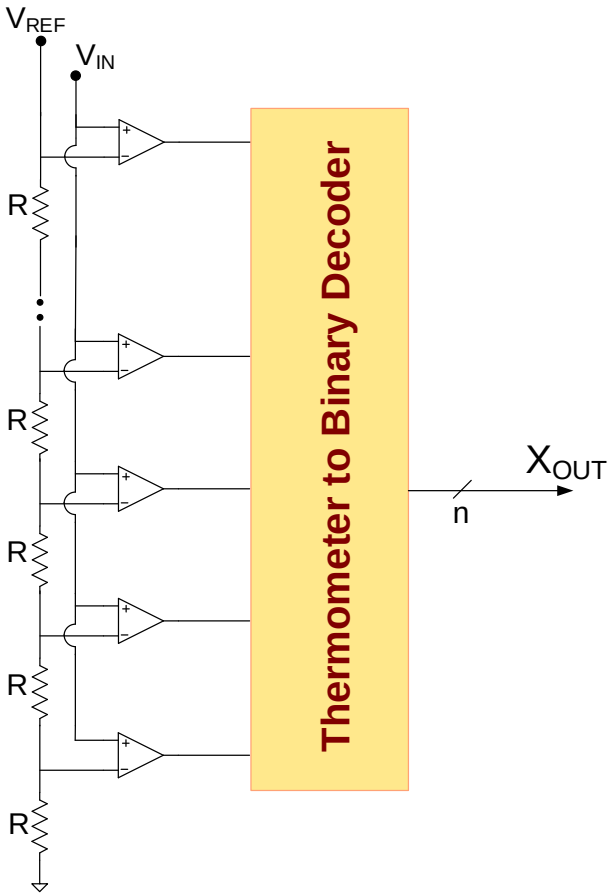
- Single-bit
- Multi-bit
- First-order
- Higher-order
- Continuous-time

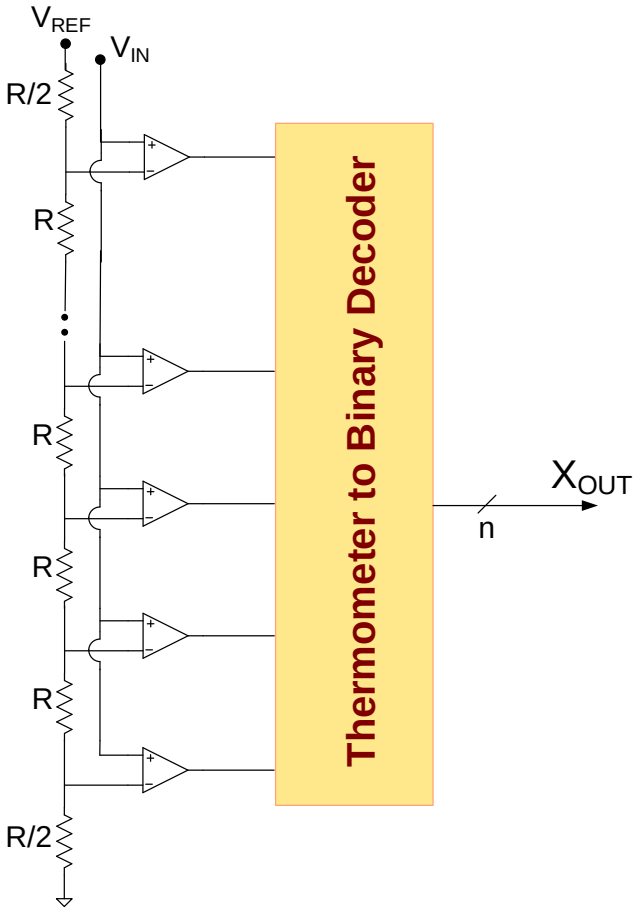
All have comparable conversion rates

Basic approach in all is very similar

Review from Last Lecture

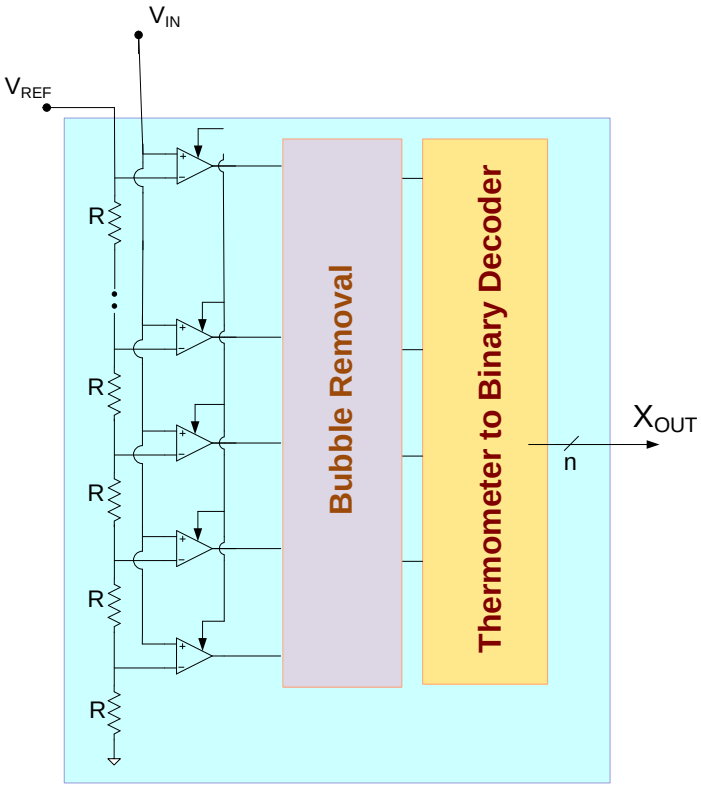
Flash ADC





Review from Last Lecture

Flash ADC



Basic structure has thermometer code at output

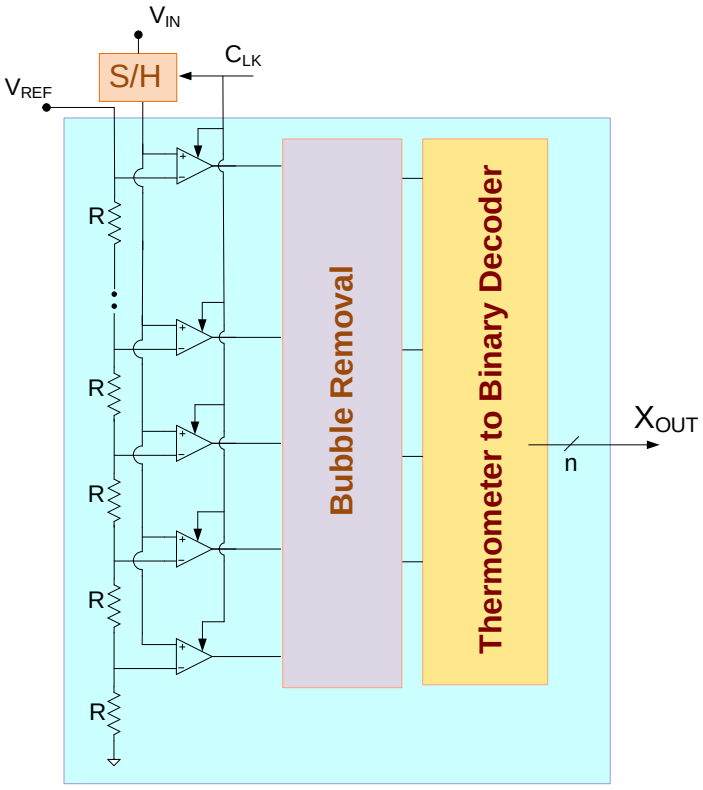
Performance Issues:

- \+ Very fast
- \+ Simple architecture
- \+ Instantaneous output

⇒ Bubble vulnerability

- − Input change during conversion
- − Offset of comparators
- − Number of components and area (for large n)
- − Speed of comparators
- − Loading of V_{REF} and V_{IN}
- − Propagation of V_{IN} and Kickback
- − Power dissipation (for large n)
- − Layout of resistors
- − Voltage and temperature dependence of R's
- − Matching of R's

Flash ADC



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- − Voltage and temperature dependence of R's
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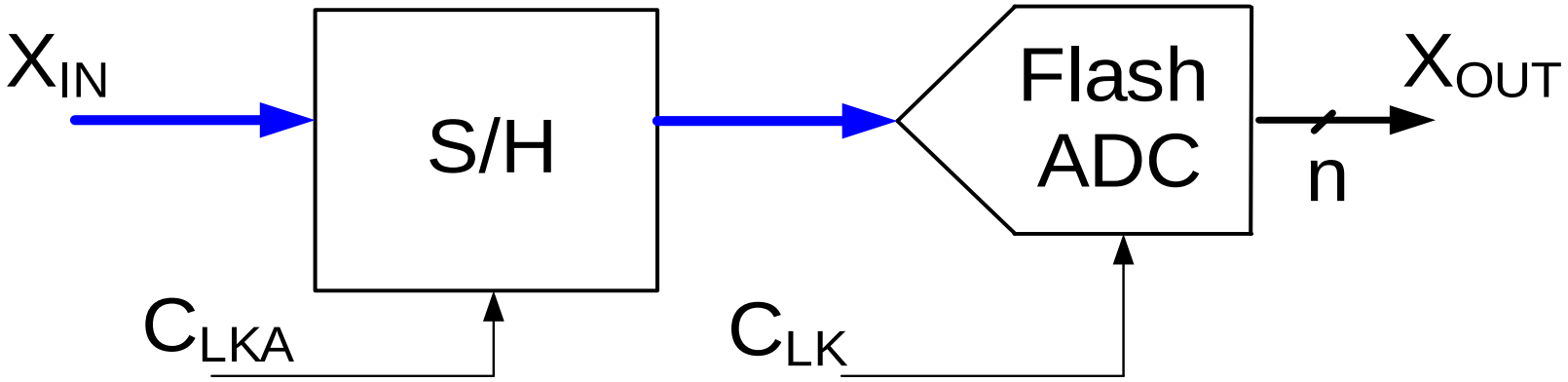
Input change during conversion

Front-End S/H can mitigate effects of input change during conversion

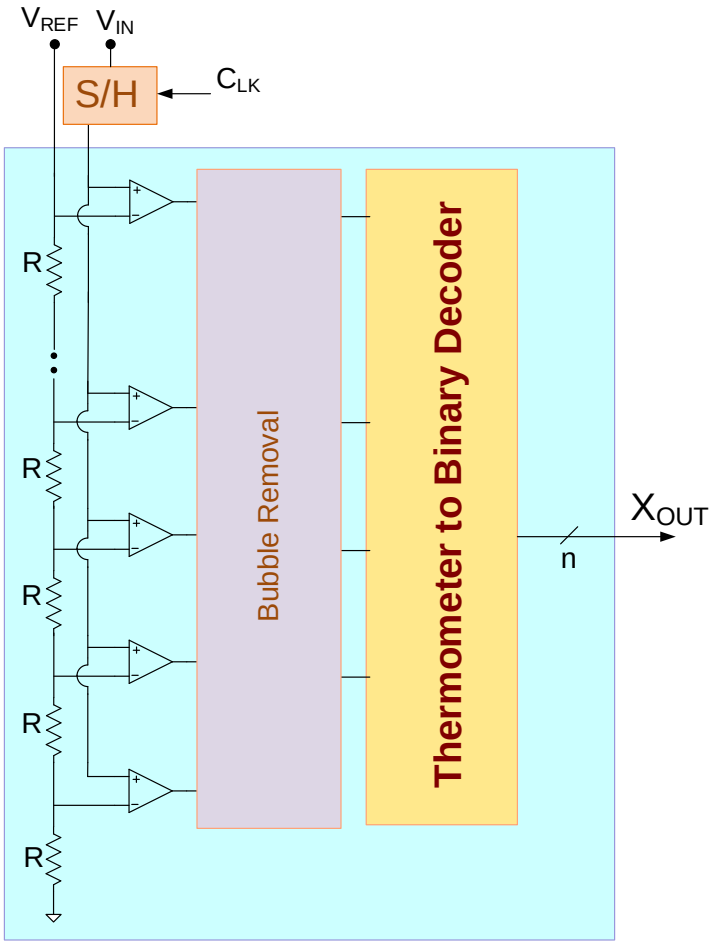


- Speed of sample/hold of concern
- Noise of S/H
- Nonlinearity of S/H
- Input range of S/H
- Power dissipation of S/H
- Loose asynchronous operation of ADC
- Widely used

⇒ S/H may be most challenging part of design

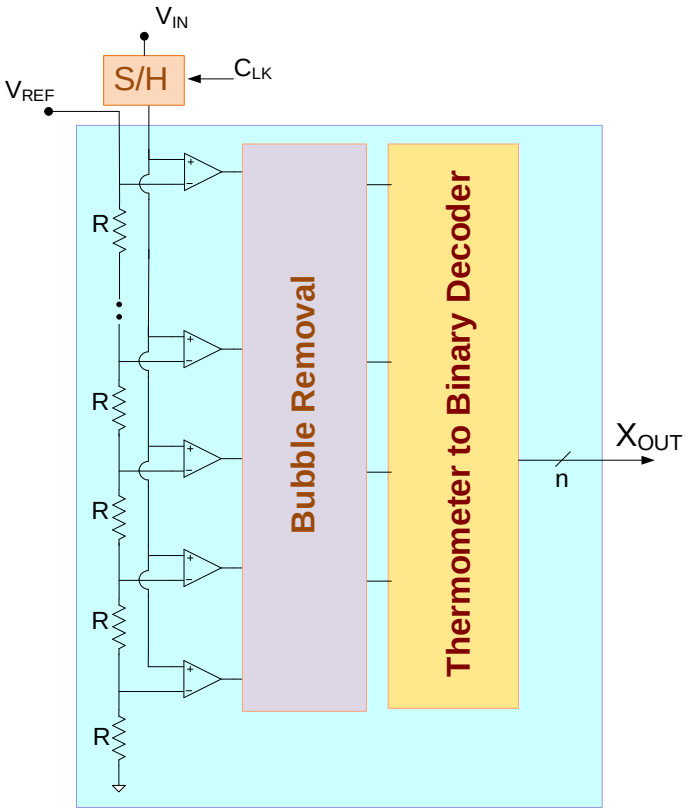
Input change during conversion

Flash ADC with Front-End S/H

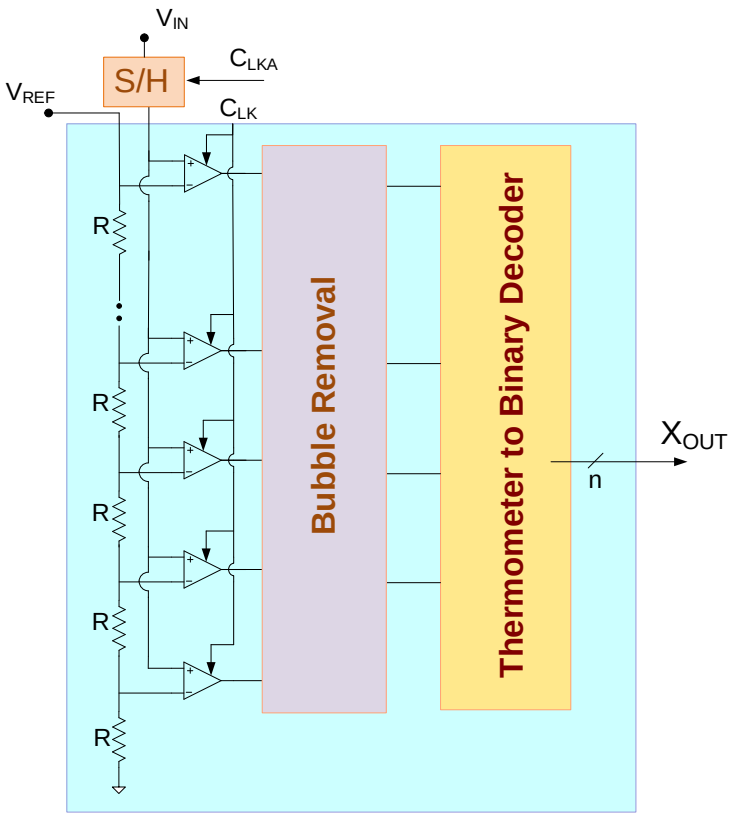


Input change during conversion

Flash ADC with Front-End S/H

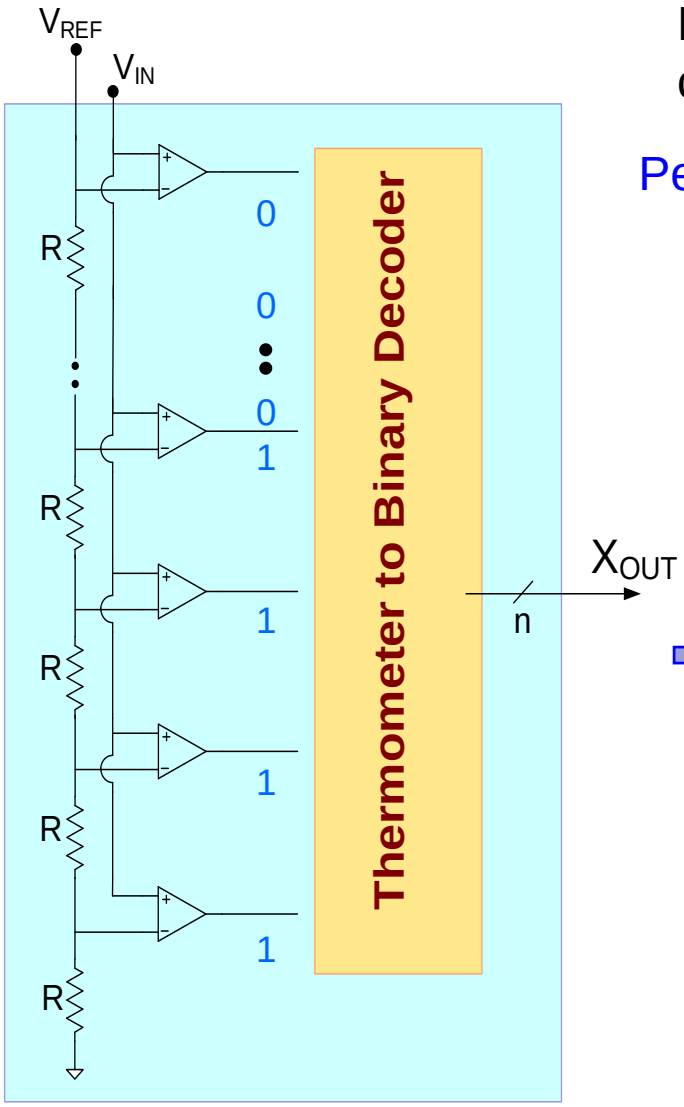


Input S/H with Clk



Input S/H with Clk and clocked comparators

Flash ADC



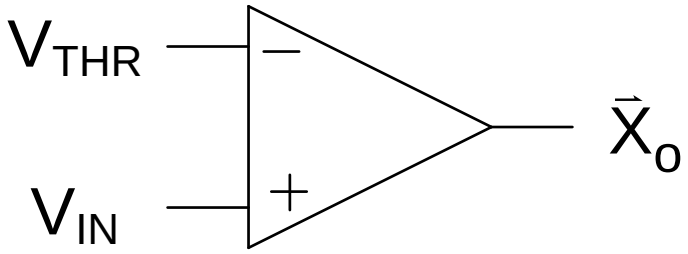
Basic structure has thermometer code at output

Performance Issues:

+ Very fast
+ Simple architecture
+ Instantaneous (asynchronous output)
+ Good DNL with low comparator offsets

− Bubble vulnerability
− Input change during conversion
− Wide range of common-mode comparator inputs
− Number of components and area (for large n)
− Loading of V_{REF} and V_{IN}
− Propagation of V_{IN}
− Power dissipation (for large n)
− Offset and speed of comparators
− Layout of resistors
− Voltage and temperature dependence of R's
− Matching of R's

Comparator



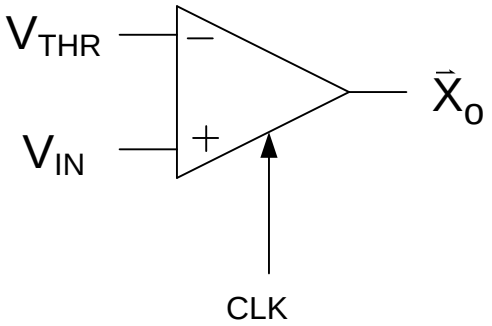
High gain amplifiers are often used as comparators since the outputs of most amplifiers naturally clip at high and low levels when overdriven

Since comparators are usually not used with feedback, there is not a need for compensation so neither the area reduction or speed reduction penalty is incurred

Since feedback is not used, higher-order amplifiers such as cascades can be used to increase the gain of a comparator to arbitrarily high levels

If over-driven amplifiers are used for comparators, the power dissipation of these types of comparators is often high

Comparator



Some comparators are clocked and only provide an output after the transition of the clock

The value of the input to a clocked comparator is only of concern in a short time interval around the clock transition

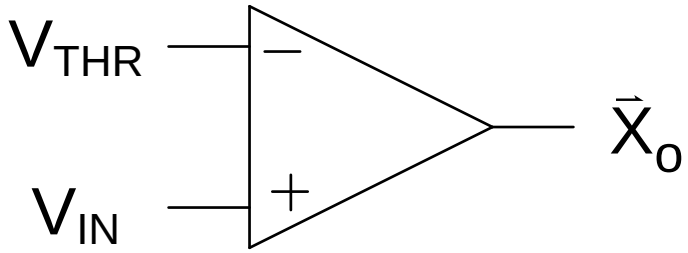
The speed of clocked comparators can be very high and the power dissipation of clocked comparators can be very low

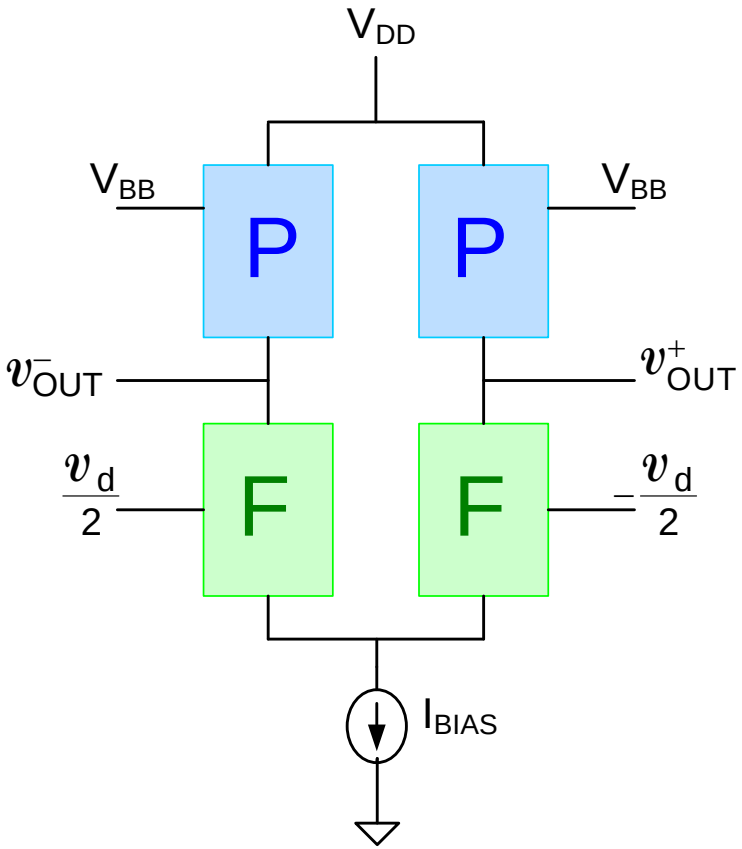
Clocked comparators are often called Dynamic Comparators

Regenerative feedback is often used in dynamic comparators and occasionally in non-clocked comparators

Dynamic comparators are widely used in the design of high-speed ADCs

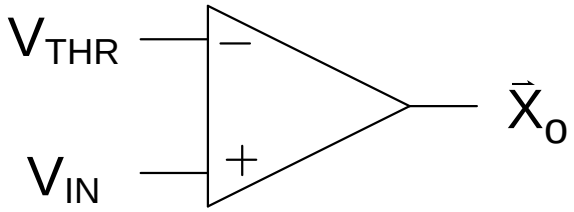
Comparator

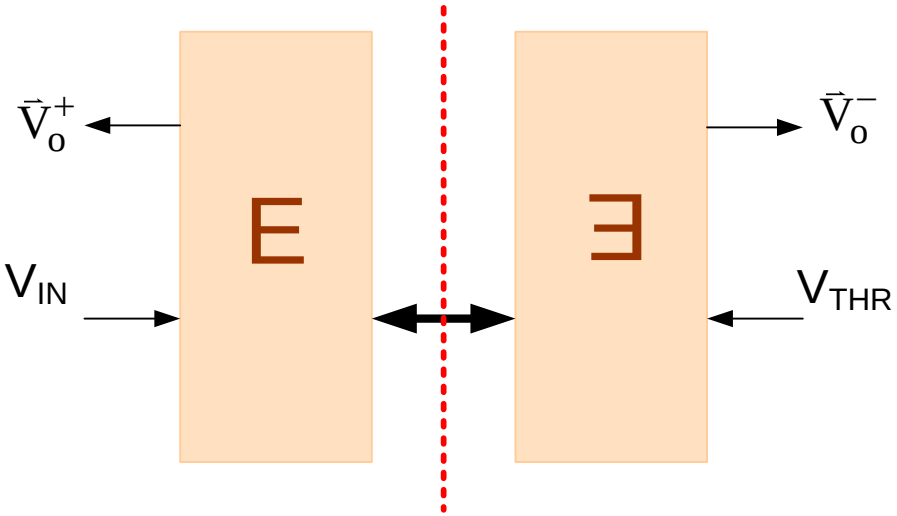




Amplifier-Based Comparator

Comparator

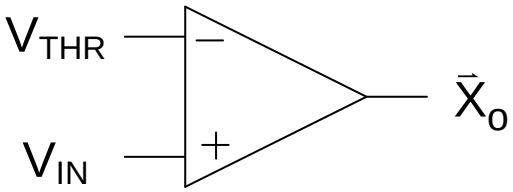


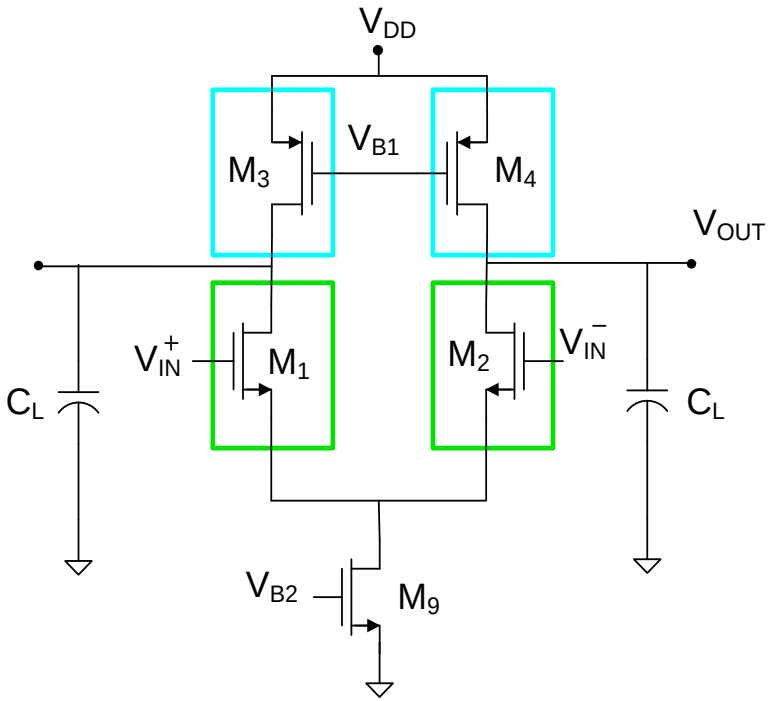


Amplifier-Based Comparator

Note symmetry in the comparator

Comparator





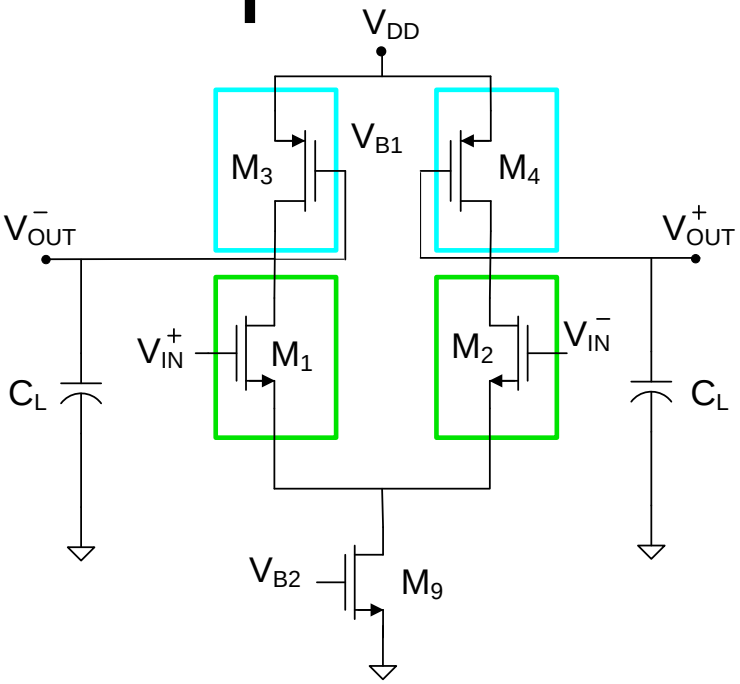
$$v_d = v_{in}^+ - v_{in}^-$$

Amplifier-Based Comparator

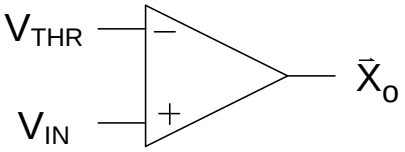
At the start of the comparison process, an amplifier-based comparator behaves as a linear amplifier

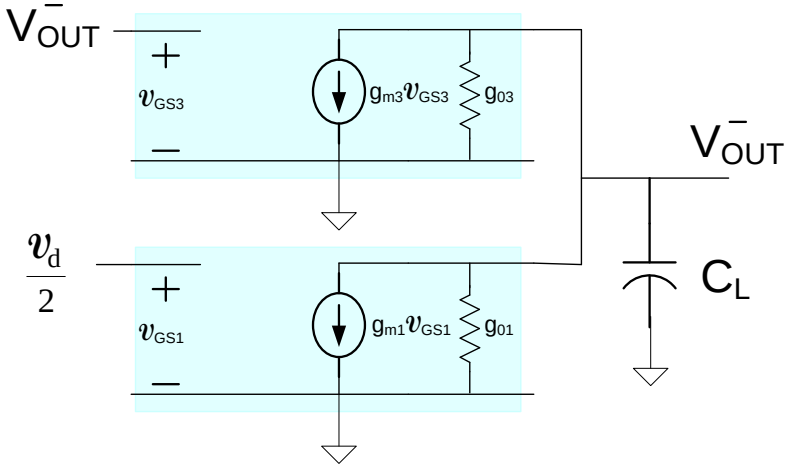
$$A(s) = \frac{v_{out}}{v_d} = \frac{1}{2}\frac{g_{m1}}{sC_L + g_{o1} + g_{o2}}$$

Comparator



$$v_d = v_{in}^{+} - v_{in}^{-}$$





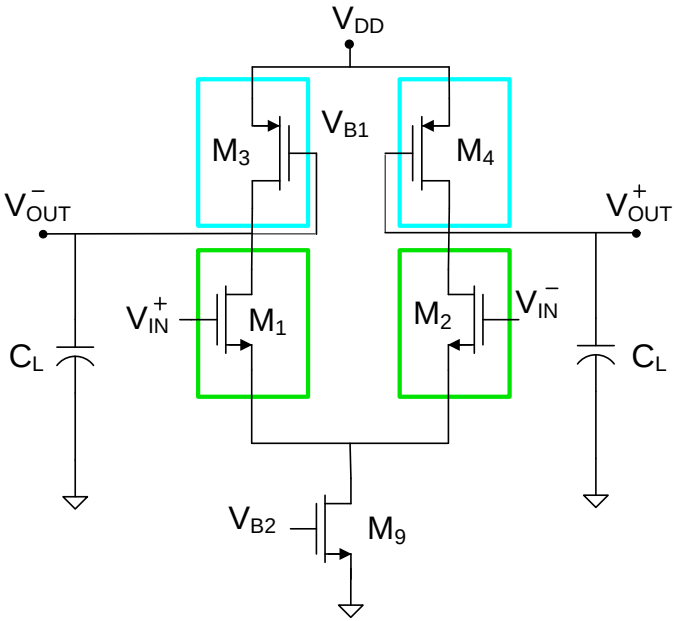
$$v_{OUT}^{-}\left(sC_L + g_{o3} + g_{o1}\right) + g_{m1}\frac{v_d}{2} + g_{m3}\left(v_{OUT}^{-}\right) = 0$$

Lower-gain Amplifier-Based Comparator

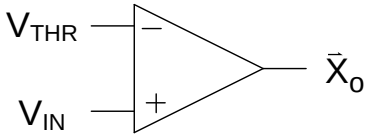
$$A(s) = \frac{v_{out}}{v_d} = -\frac{1}{2}\frac{g_{m1}}{sC_L + g_{o1} + g_{o2} + g_{m3}}$$

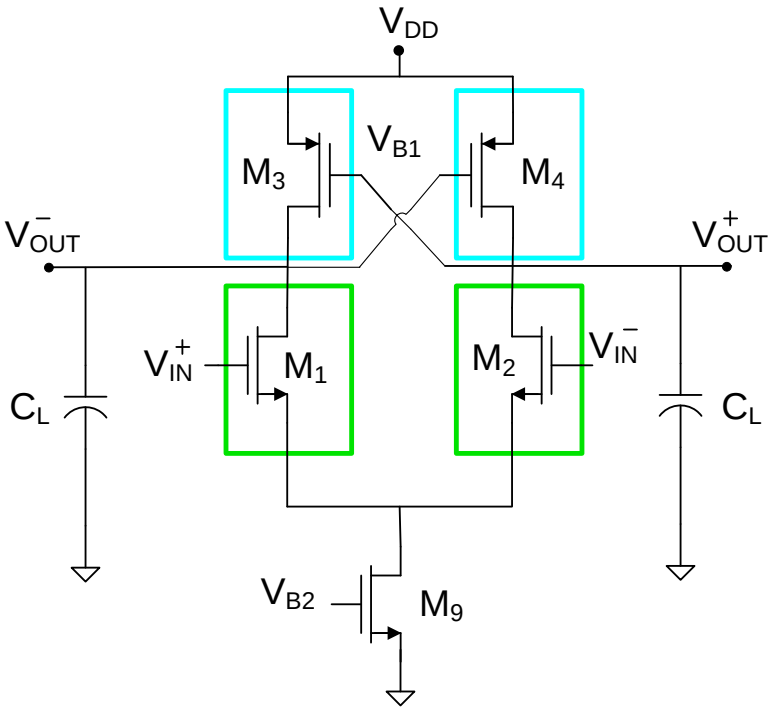
At the start of the comparison process, an amplifier-based comparator behaves as a linear amplifier

Comparator



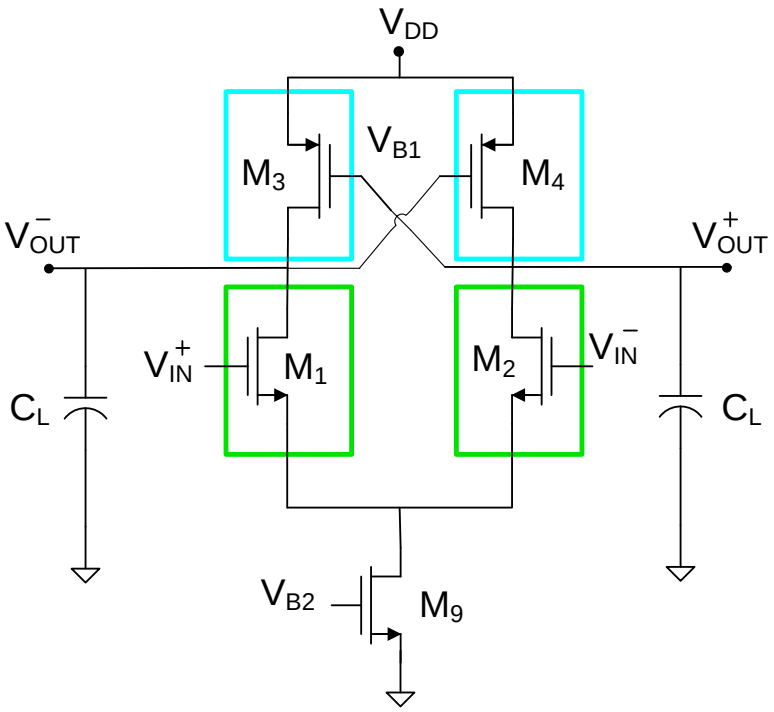
Lower-gain Amplifier-Based Comparator





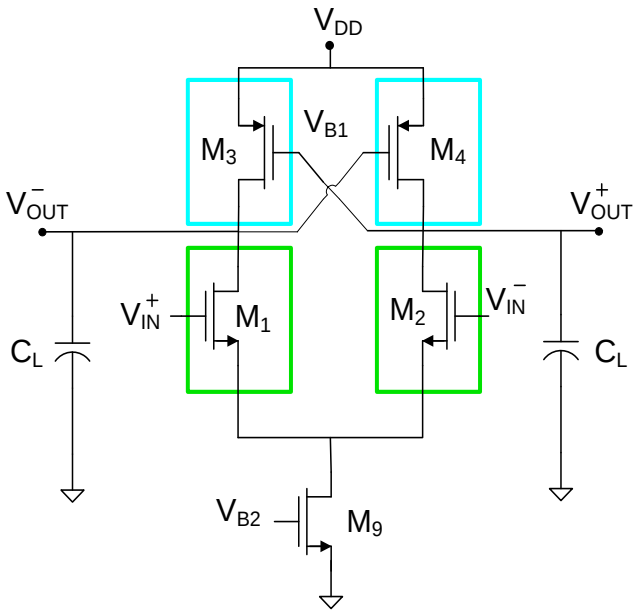
Amplifier-Based Comparator with Regenerative Feedback

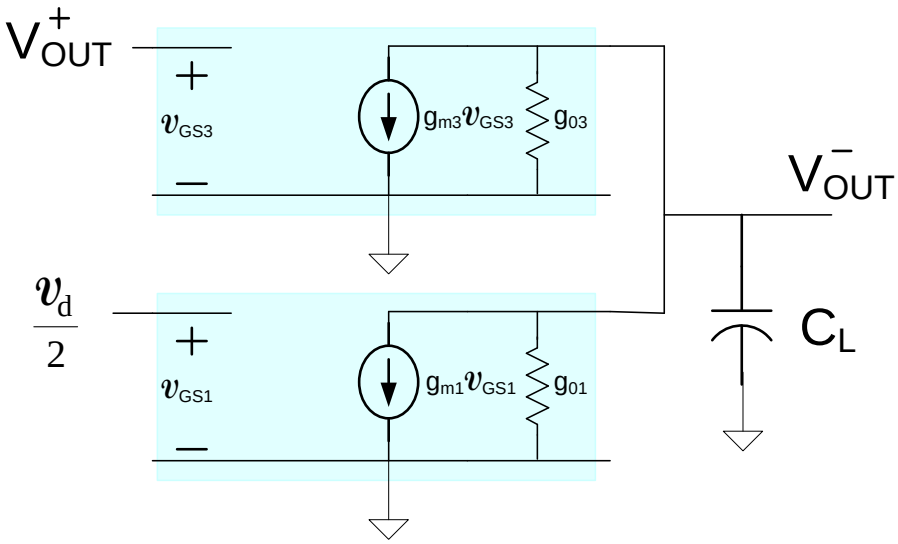
Amplifier-Based Comparator with Regenerative Feedback



At the start of the comparison process, an amplifier-based comparator behaves as a linear amplifier

Amplifier-Based Comparator with Regenerative Feedback





At the start of the comparison process, an amplifier-based comparator behaves as a linear amplifier

$$v_{OUT}^{-}\left(sC_L + g_{o3} + g_{o1}\right) + g_{m1}\frac{v_d}{2} + g_{m3}\left(-v_{OUT}^{-}\right) = 0$$

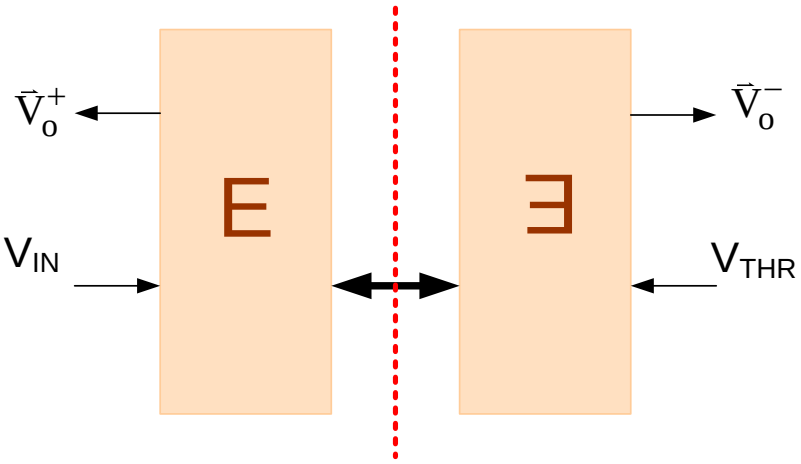
$$\frac{v_{OUT}^{-}}{v_d} = \frac{-\frac{g_{m1}}{2}}{sC_L + g_{o3} + g_{o1} - g_{m3}}$$

Since $g_m >> g_o$, this comparator has a pole on positive real axis in the RHP

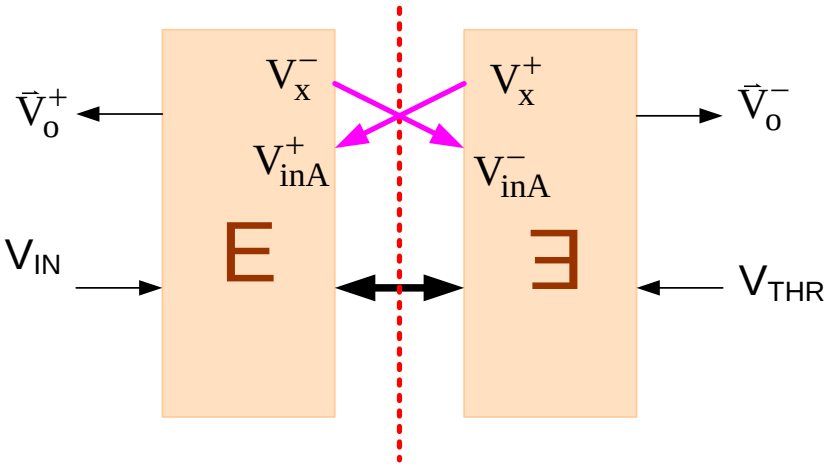
Regenerative feedback will cause the output to latch at one of two levels

But will not recover if small changes in input dictate a change in the output

Comparator Structures



Amplifier-Based Comparator



Comparator with Regenerative Feedback

Almost all comparators based upon two symmetric sub-circuits

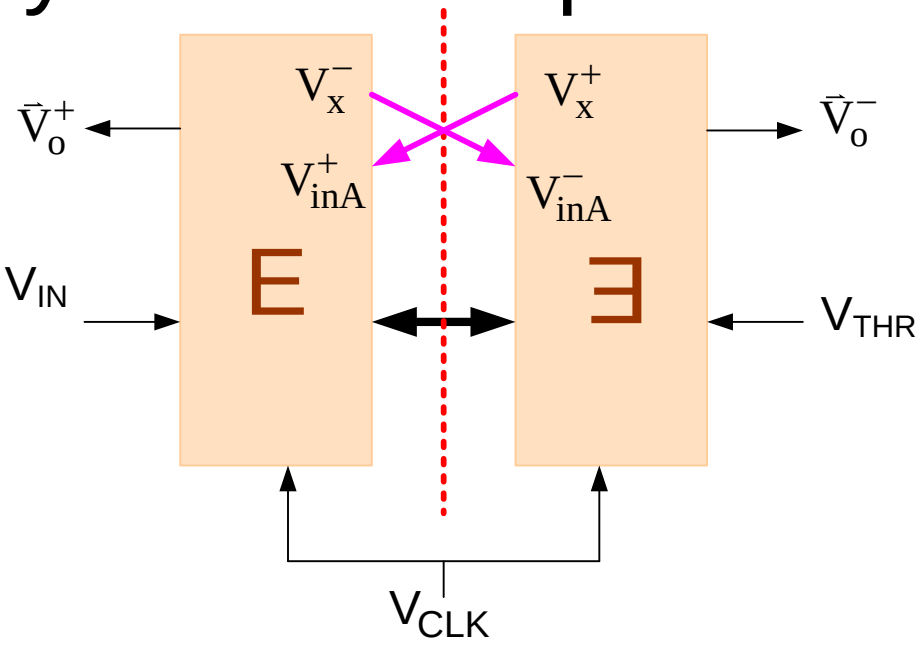
Regeneration obtained by symmetrically cross-coupling across axis of symmetry from an output to an input

Any symmetric structure with this cross-coupling will create regenerative feedback but whether the poles move into the RHP depends upon the architecture

Clocks are often added to remove the restriction of regenerative-type structures not recovering when inputs change a little

Structure in upper right will be called a “Cross-Symmetric” structure

Generic Dynamic Comparator Structure

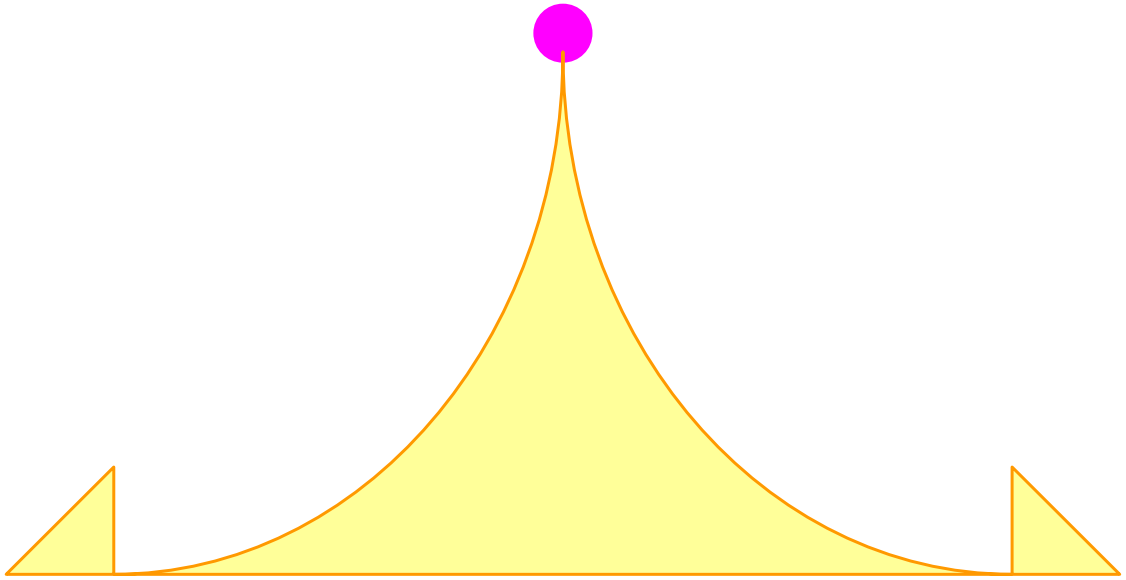


Most circuits with this architecture that have a modest regenerative feedback gain will have a RHP positive real axis pole

All circuits with the cross-symmetric structure and a positive real axis pole can serve as dynamic comparators!

The clock is used to reset the circuit and thus to put it in a balanced state prior to regeneration

Mechanical Analogy of Dynamic Comparator

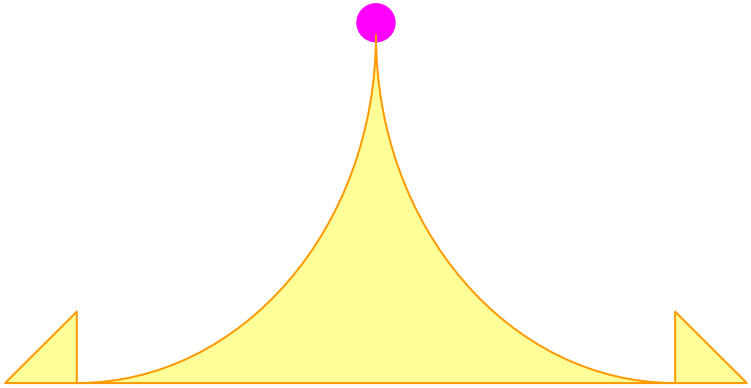


Ball in position shown is said to be in a metastable state

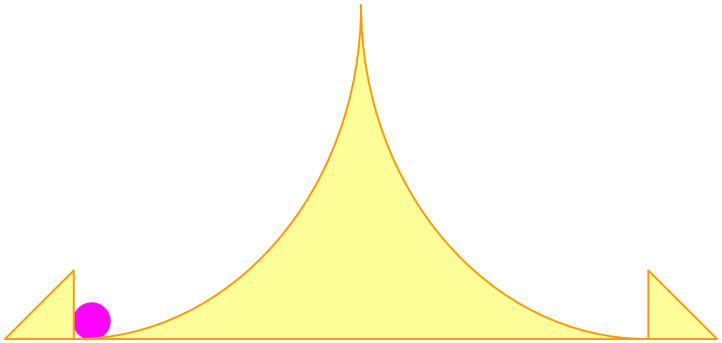
This system can not stay in this state indefinitely

A “reset” must be applied to put the system in the metastable state

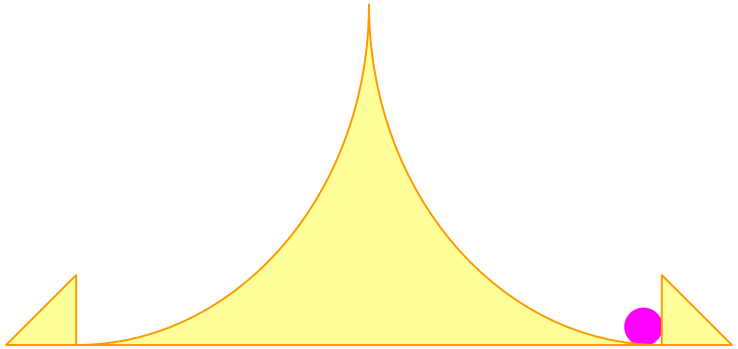
Mechanical Analogy of Dynamic Comparator



Metastable State



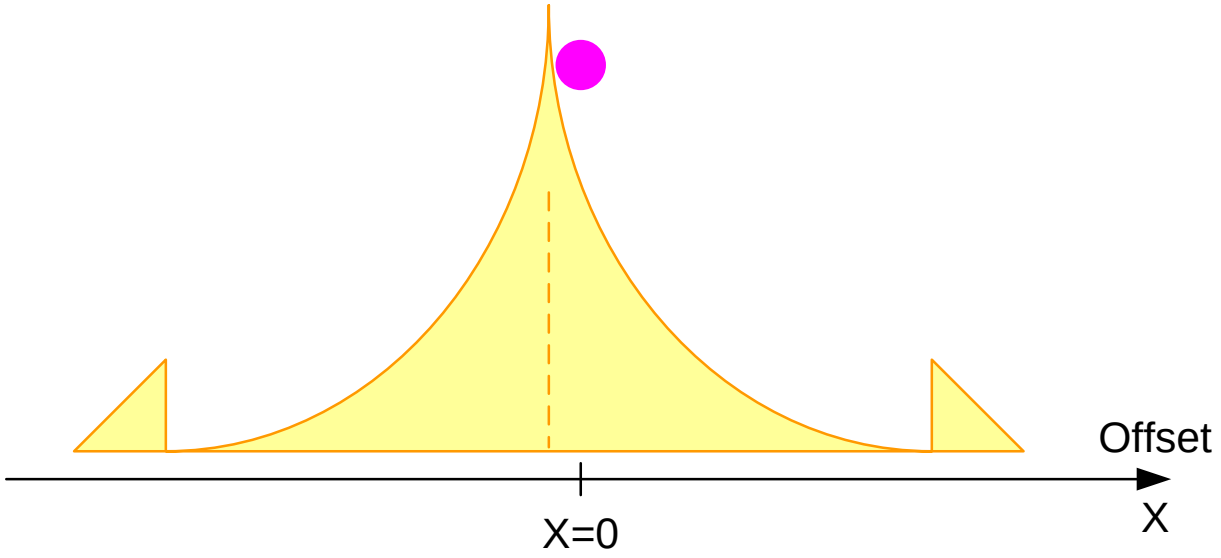
Left Stable State



Right Stable State

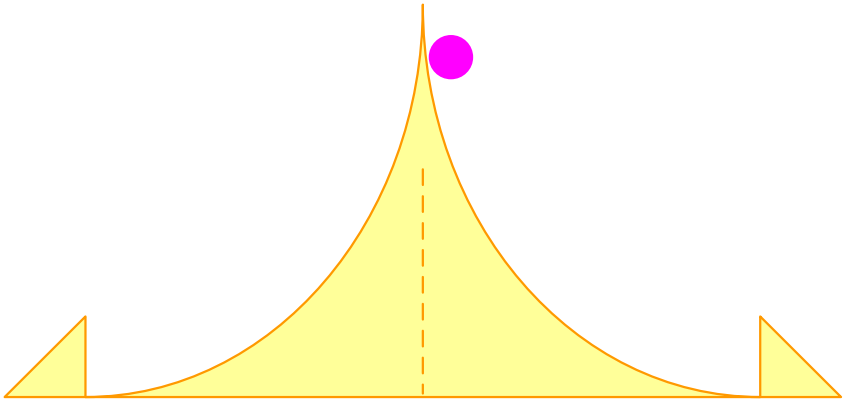
- Given enough time, system will always enter one of the two stable states
- Time required to enter one of the two stable states is usually very small

Mechanical Analogy of Dynamic Comparator



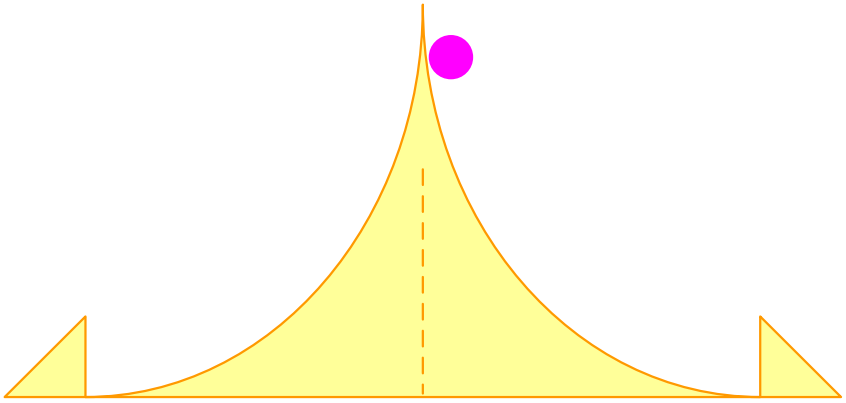
- If at reset (ball at position x=0) the system is offset a small amount, a stable state will be reached very quickly
- Time required to enter one of the two stable states is usually very small
- The state it reaches tells whether the system offset is positive or negative
- The position of the ball after a small period of time provides a “boolean” output that gives the result of the comparison between the position of the ball and the position of the system
- This thus serves as a mechanical dynamic comparator

Mechanical Analogy of Dynamic Comparator



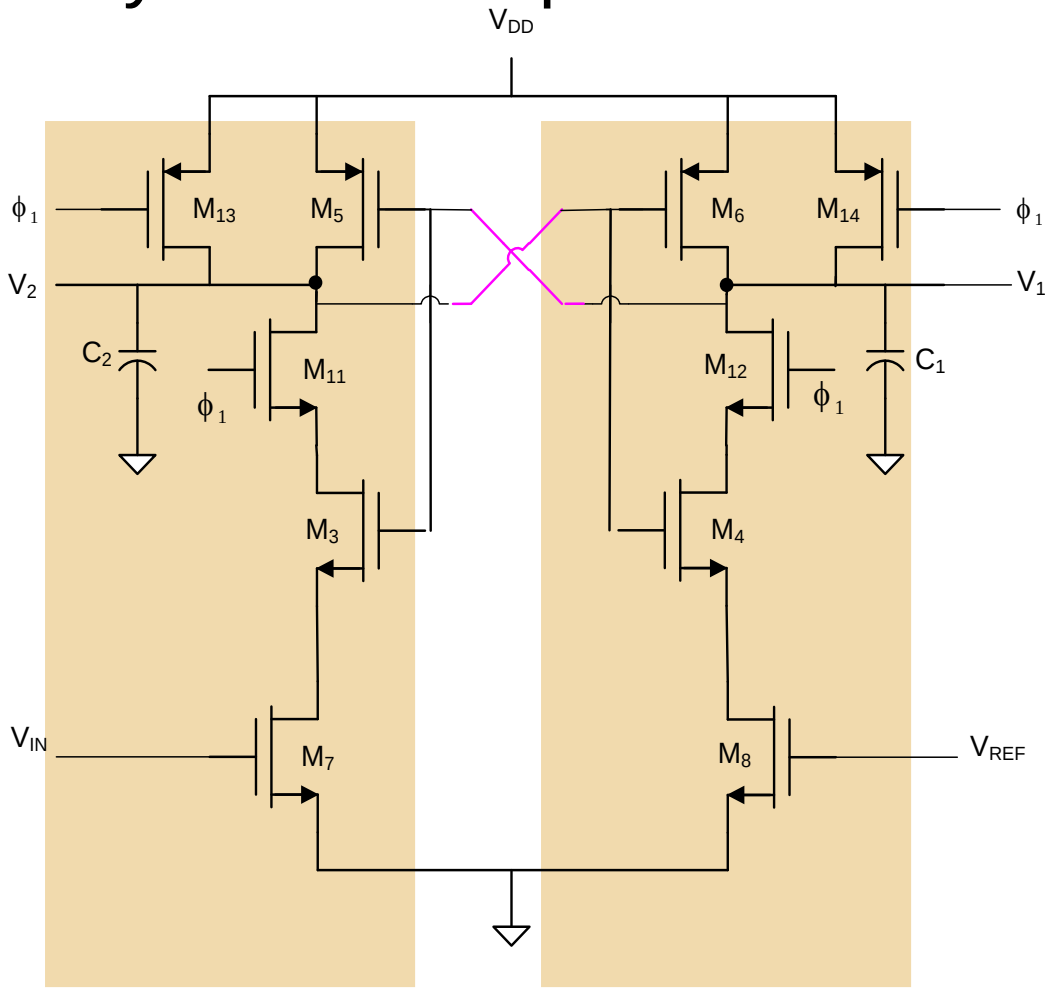
- Probability is 0 of having the initial offset be exactly 0
- Dynamic comparator will always make a decision
- But, if the offset is sufficiently close to 0, it may take a long time to make a decision
- In this mechanical system, the time it takes to make a decision is dependent upon the geometry of the system, the mass of the ball, and the coefficient of friction

Mechanical Analogy of Dynamic Comparator



- If the initial offset is uniformly distributed around x=0, for any time t, there is a small probability that the decision will not have been made at time t
- This probability is large if t is very small and is very small if t is large
- Some authors refer to the system being in a “metastable” state when a decision has not been reached but this term is misleading.
- If at any time t, the comparator has not made a decision, the system is in a transition state
- Most useful circuits that serve as dynamic comparators are very fast – that is, they have a very high probability of making a decision in a very short time

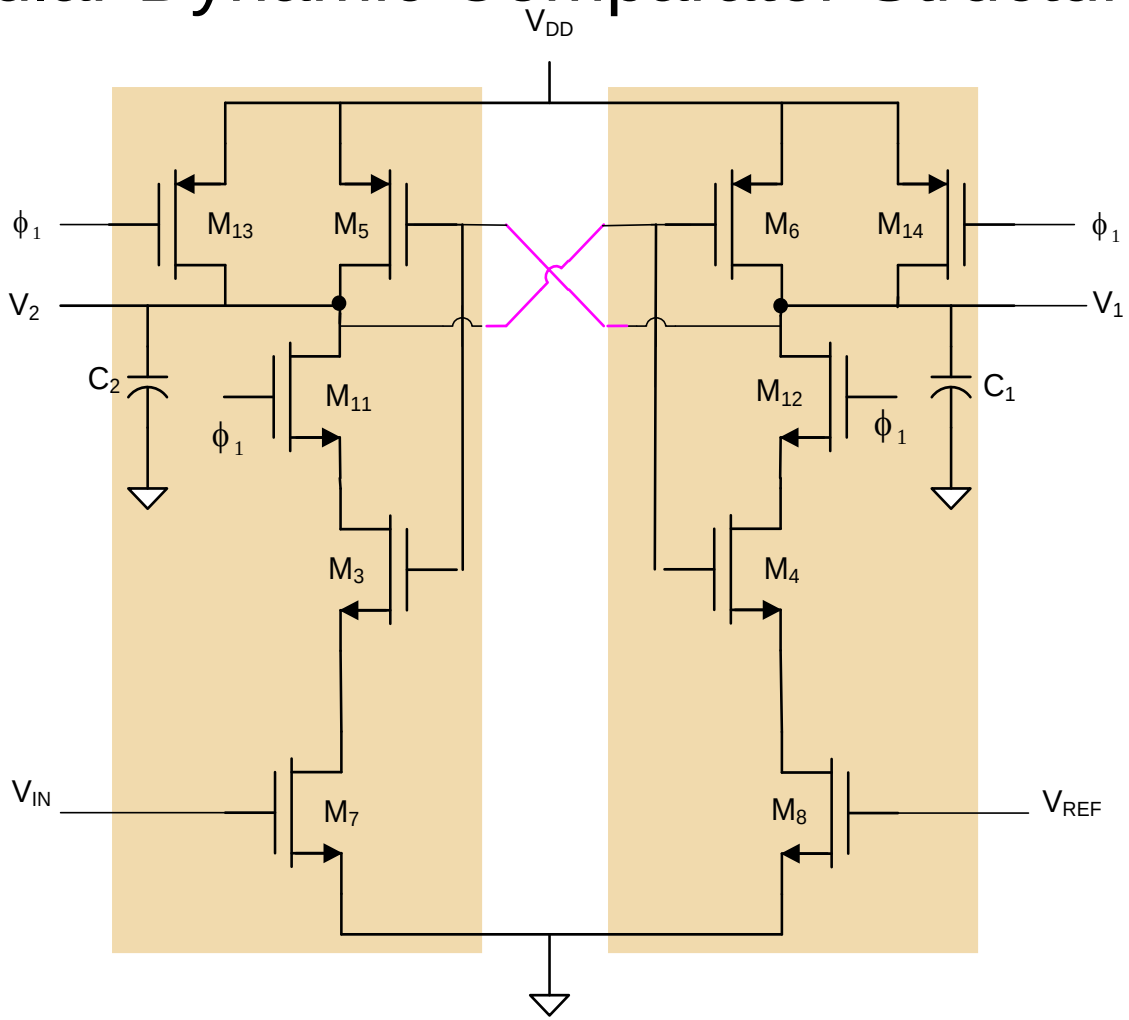
Popular Dynamic Comparator Structure



Brief discussion of operation:

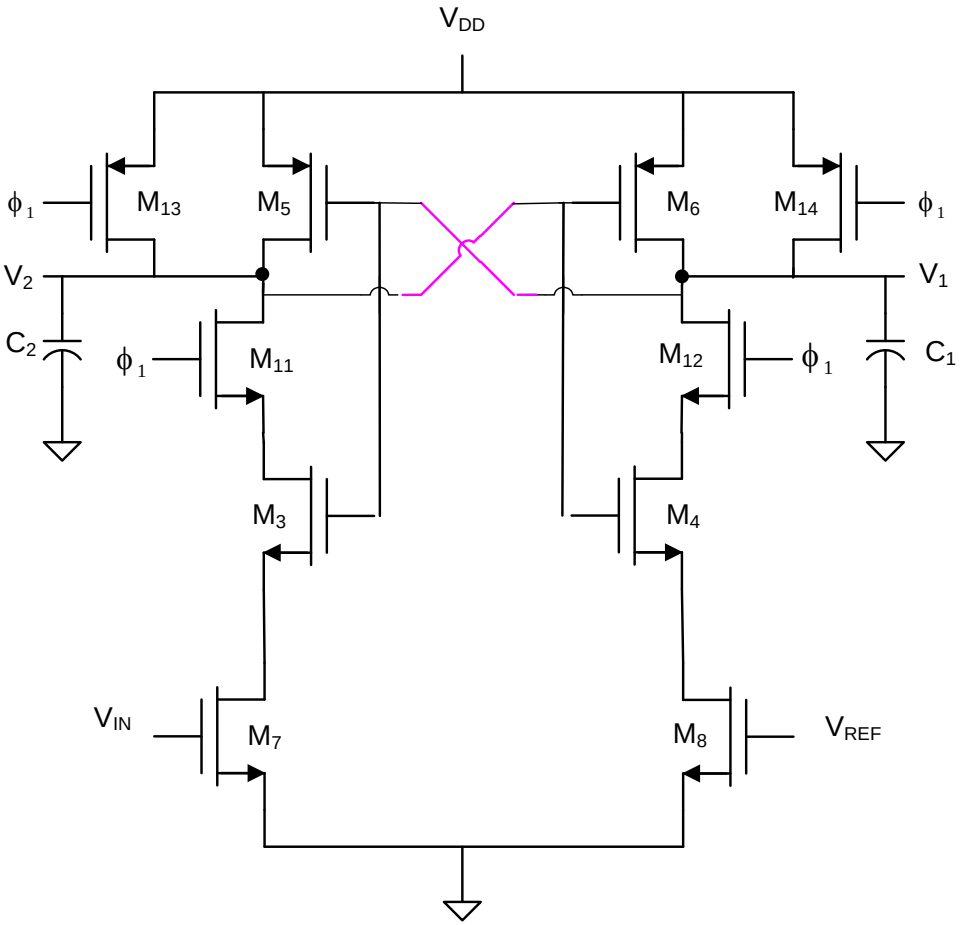
If $V_{IN}>V_{REF}$ at the start of the evaluate state, the current in M_7 will increase more rapidly than the current in M_8. Hence the current in M_5 will cause the magnitude of V_{GS} on M_5 to increase. This drives V_1 down and ultimately V_2 up

Popular Dynamic Comparator Structure



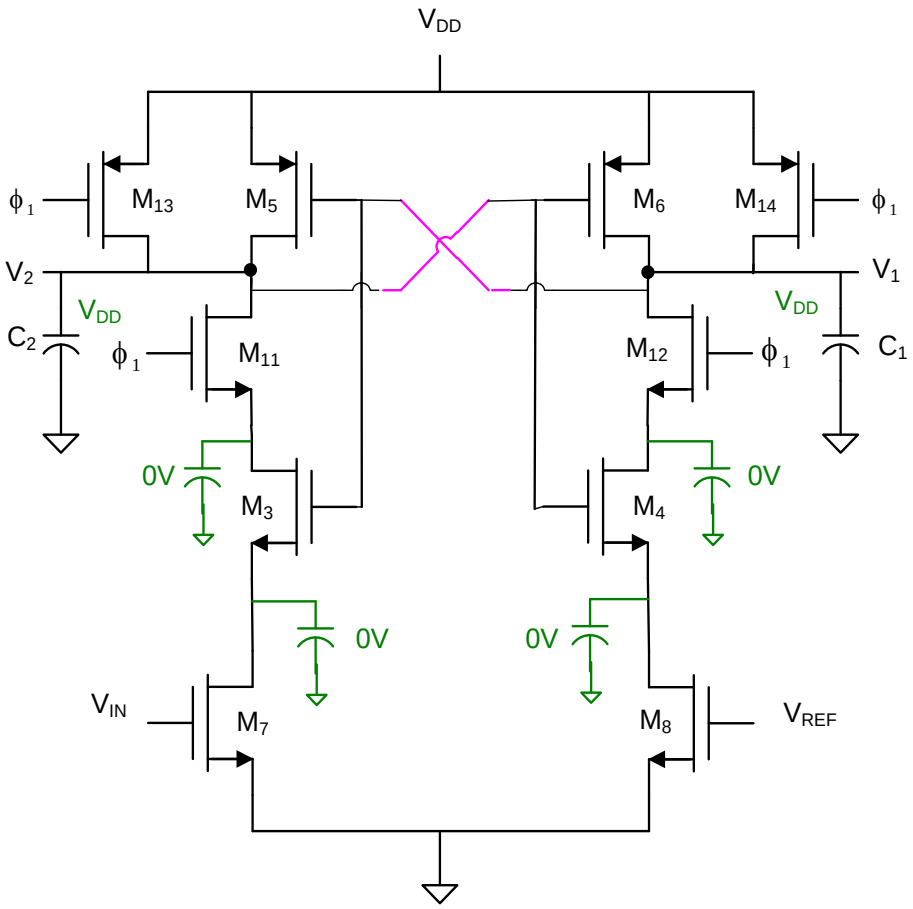
Load can be viewed as two cross-coupled Boolean inverters
Note zero static power dissipation

Popular Dynamic Comparator Structure



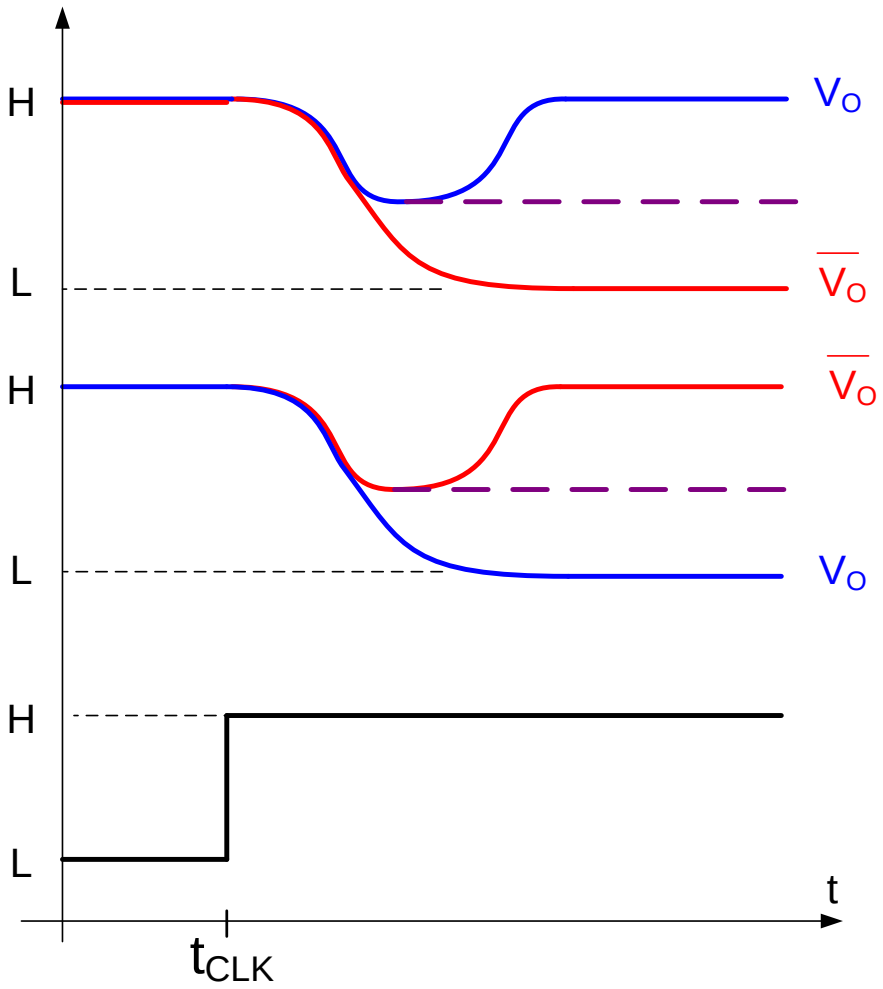
- Load can be viewed as two cross-coupled Boolean inverters
- Note zero static power dissipation !

Popular Dynamic Comparator Structure

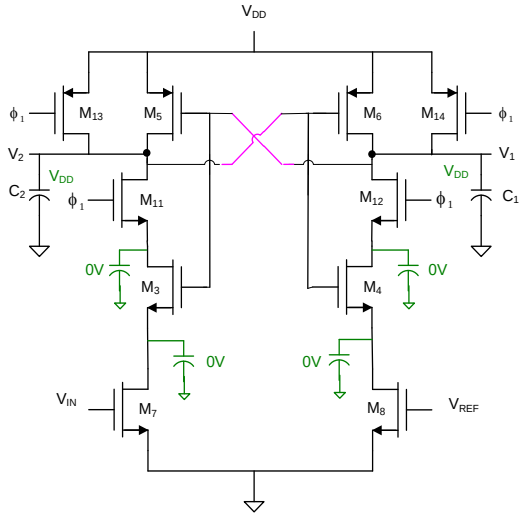


- Reset precharges
  - V_1 and V_2 to V_{DD}
  - the voltage on the source node of M_1 to 0V
  - The volgate on the source node of M_3 to 0V
- Note zero static power dissipation !

Popular Dynamic Comparator Structure



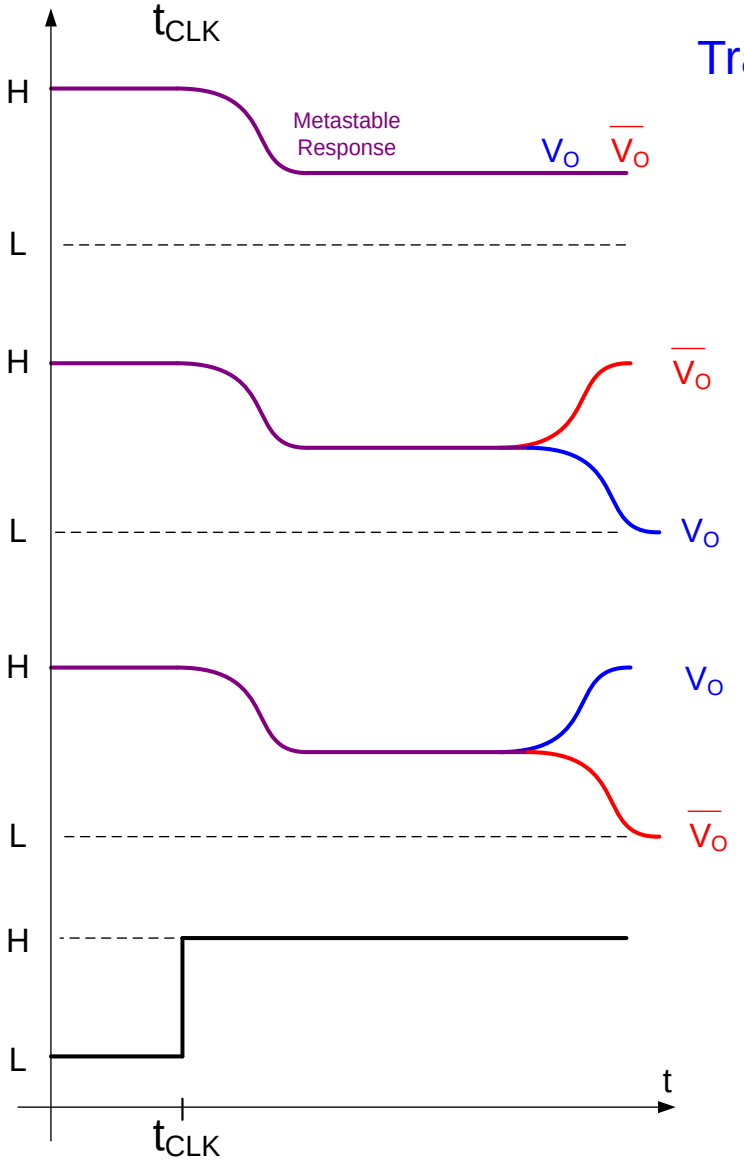
Transient Response

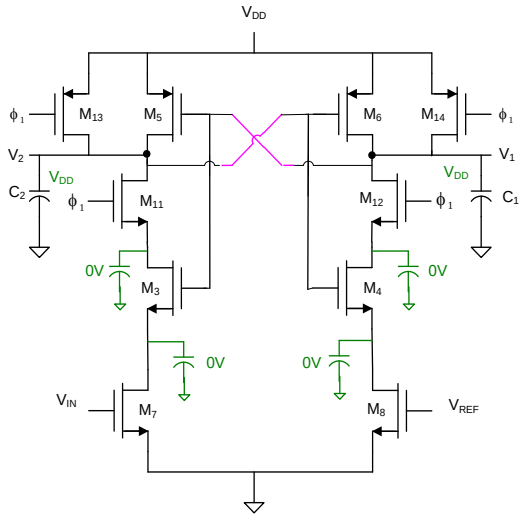


Note: Both outputs always start high and then transition

Popular Dynamic Comparator Structure

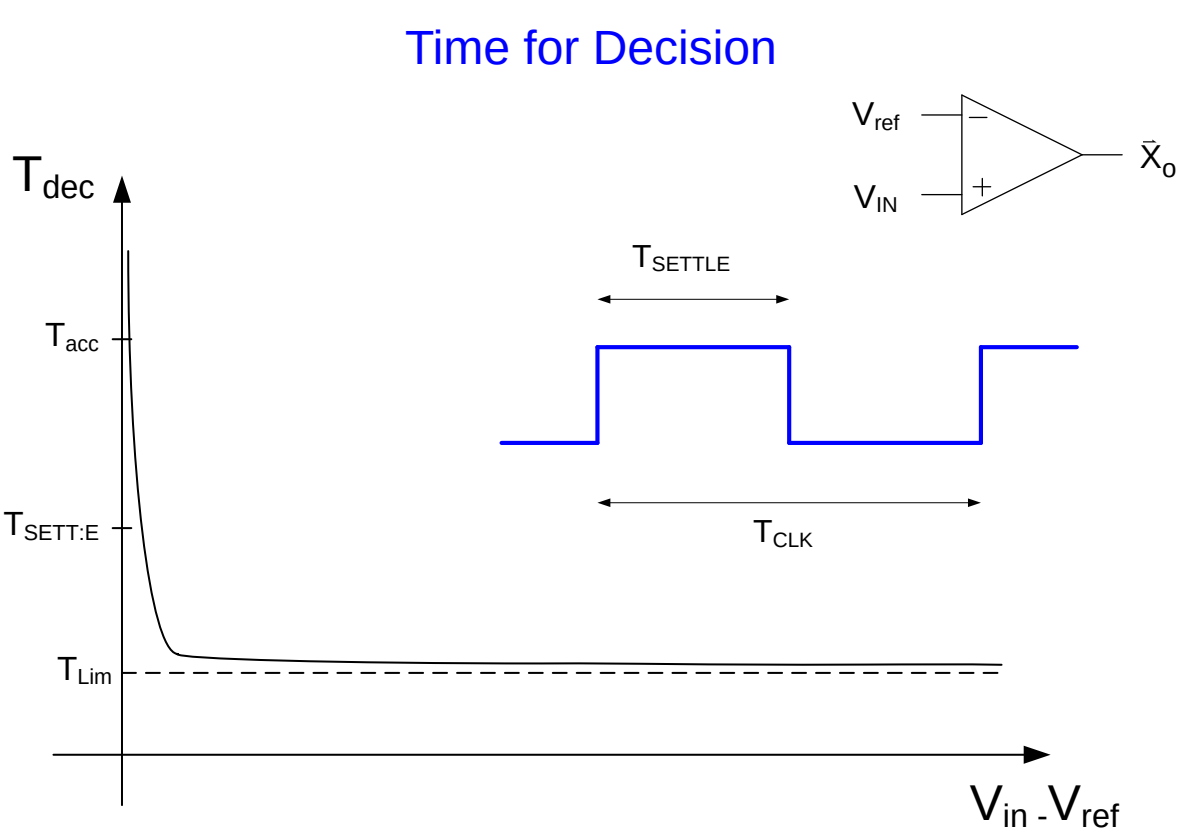
Transient Response

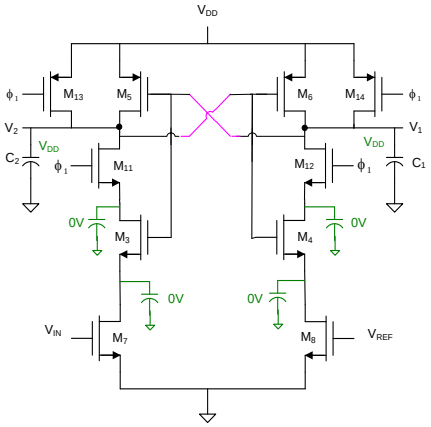




Note: Will always leave metastable region but will occasionally not leave region soon enough

Popular Dynamic Comparator Structure

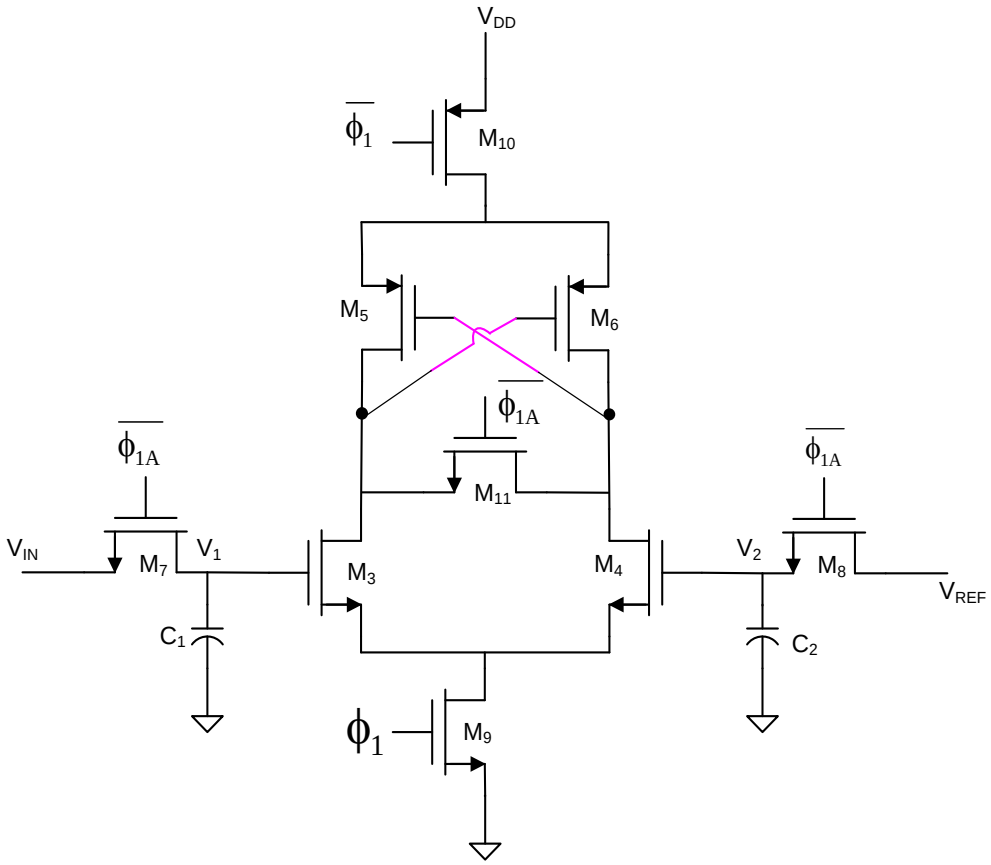




T_{acc} is the maximum clock settling period that will give an acceptable probability of error in a comparator

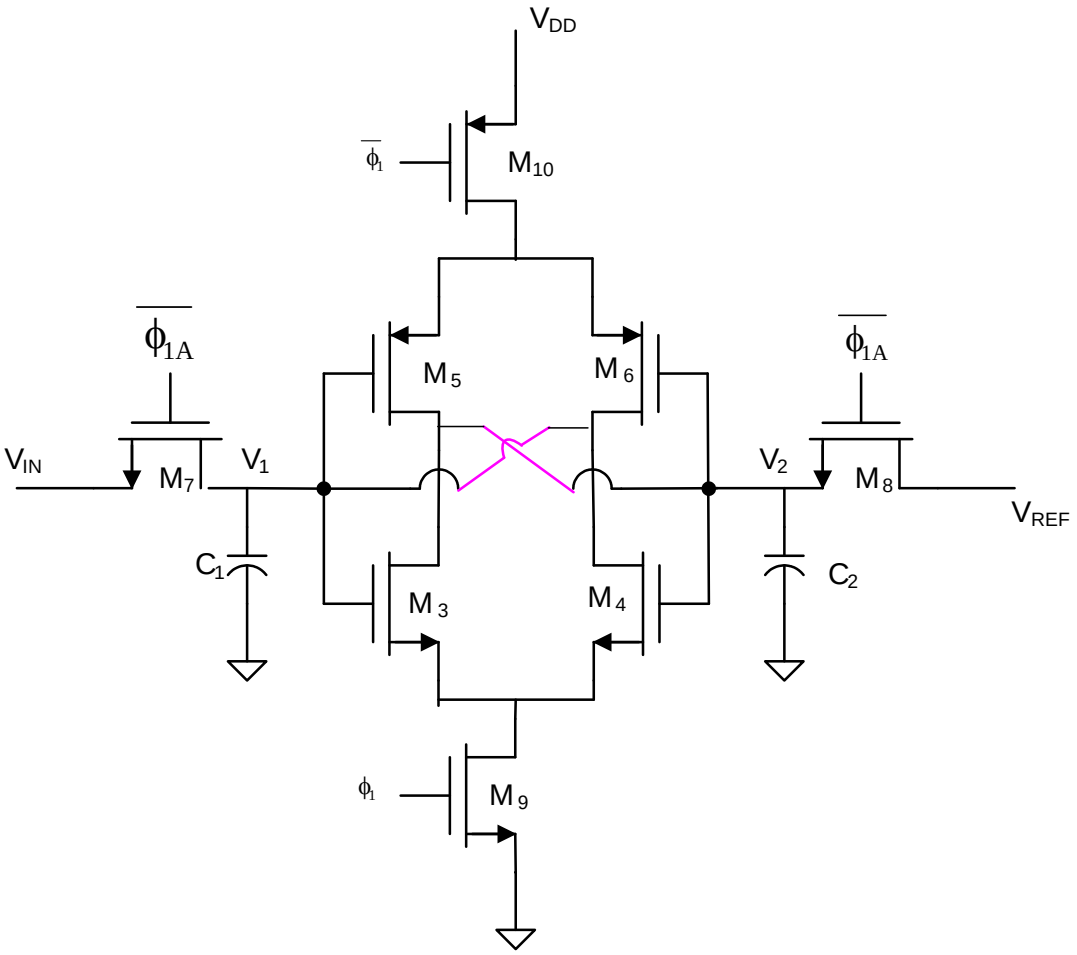
T_{Lim} is the limit of the settling time as the overdrive becomes large

Popular Dynamic Comparator Structure



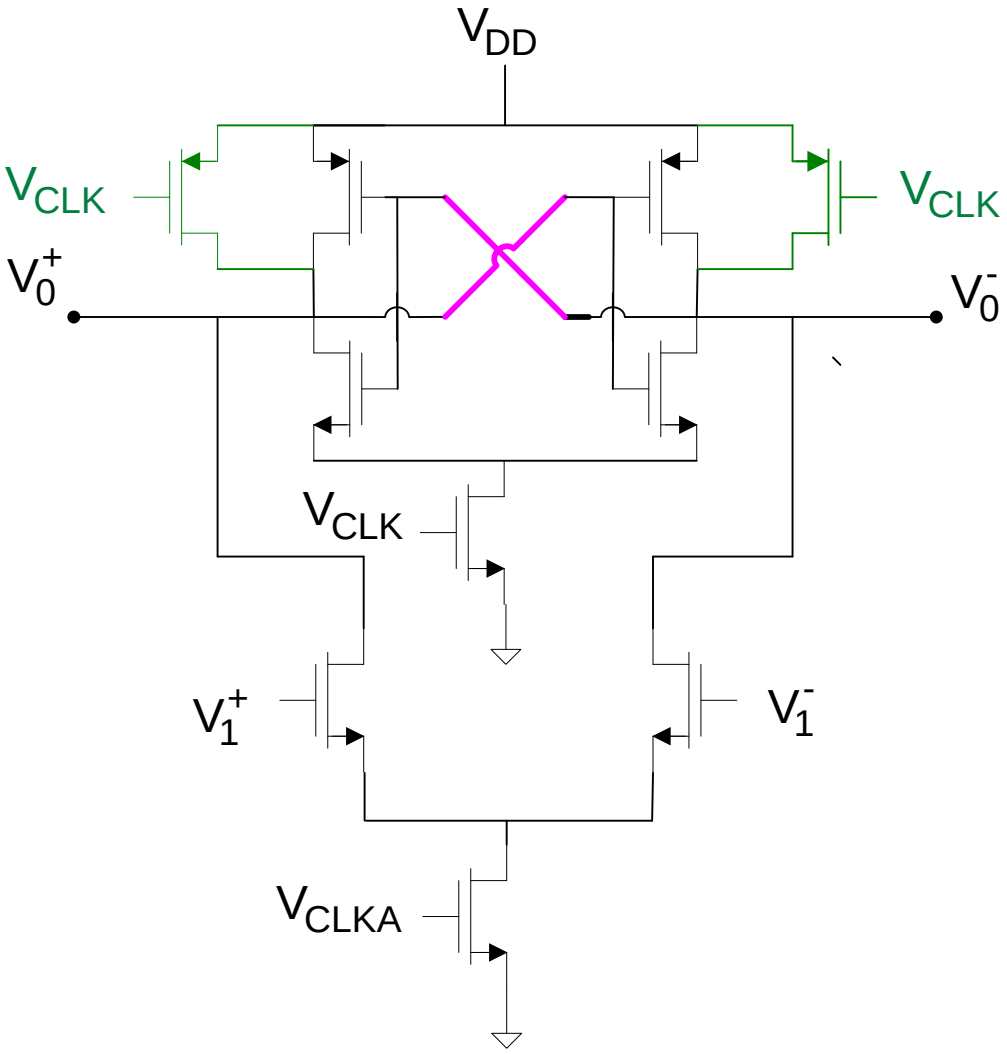
- Note zero static power dissipation in the “arm” state !

Popular Dynamic Comparator Structure



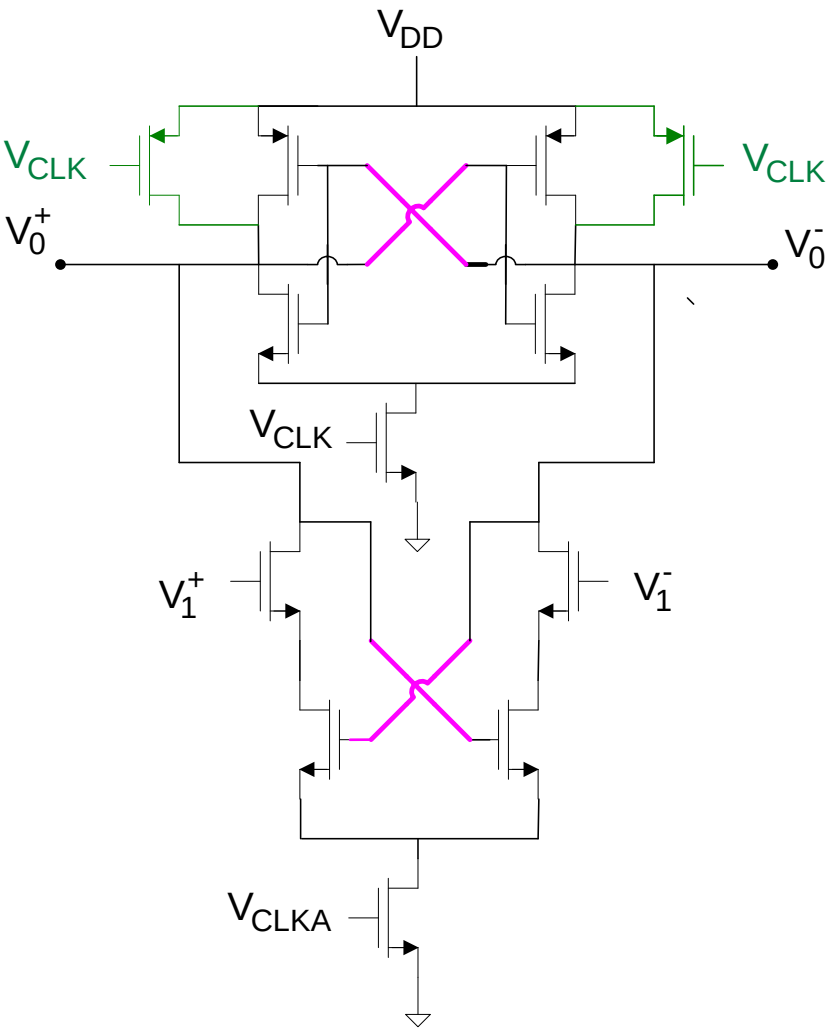
- Reset sets inverter pair at trip point
- Note zero static power dissipation !

Popular Dynamic Comparator Structure



- Note zero static power dissipation !

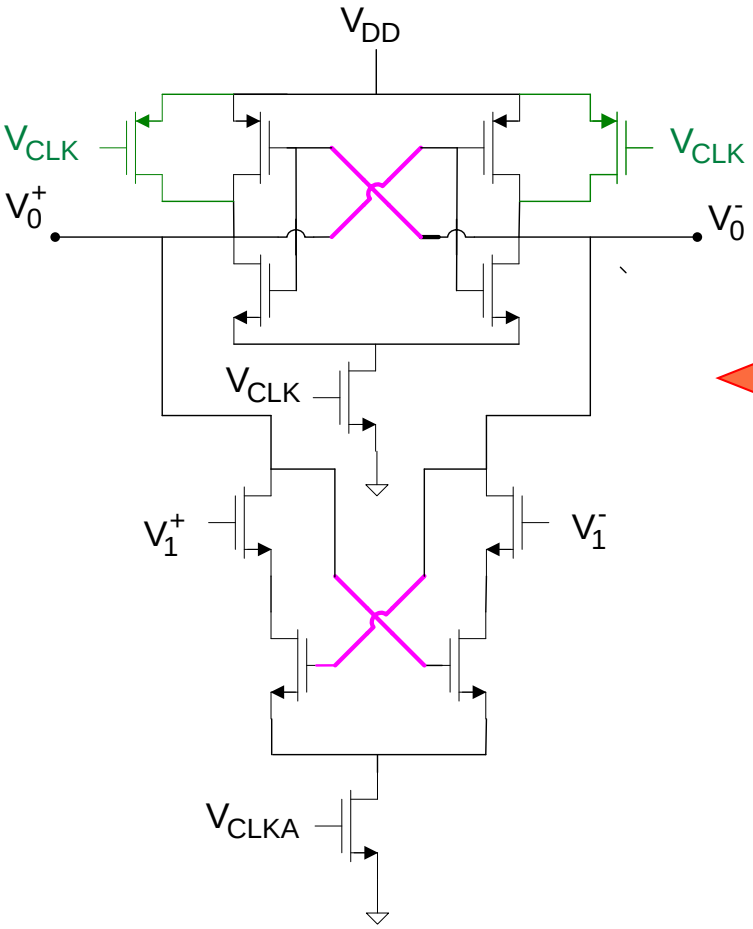
Popular Dynamic Comparator Structure



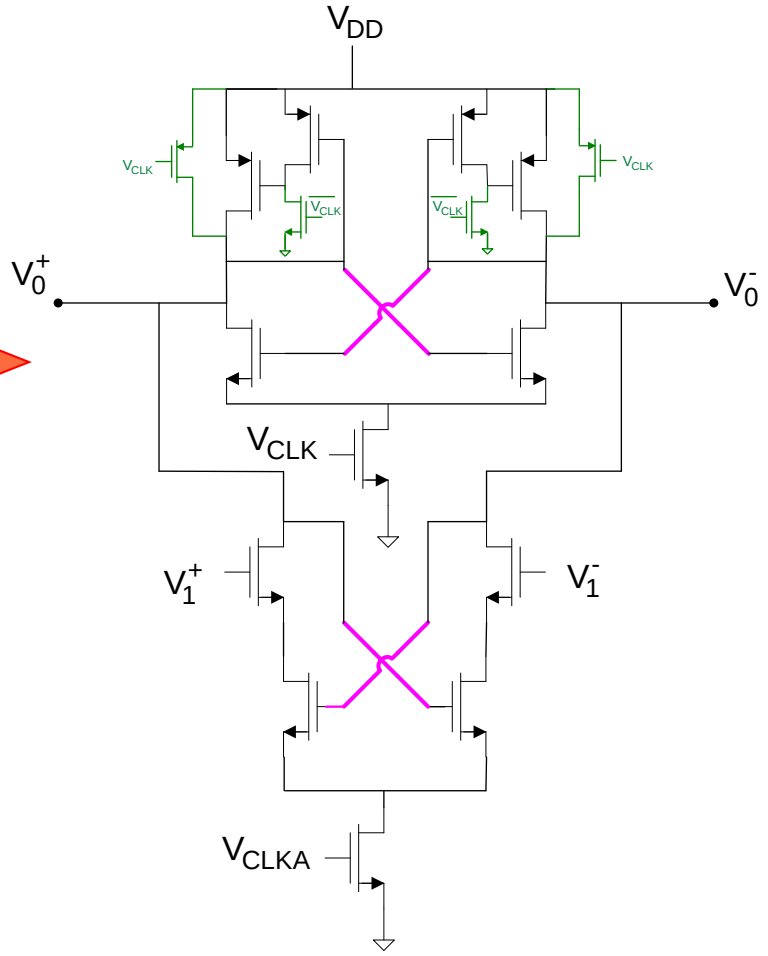
Goff ISSCC 2009 (maybe not original source)

Alternate Dynamic Comparator Structure

How does this compare with the previous structure?

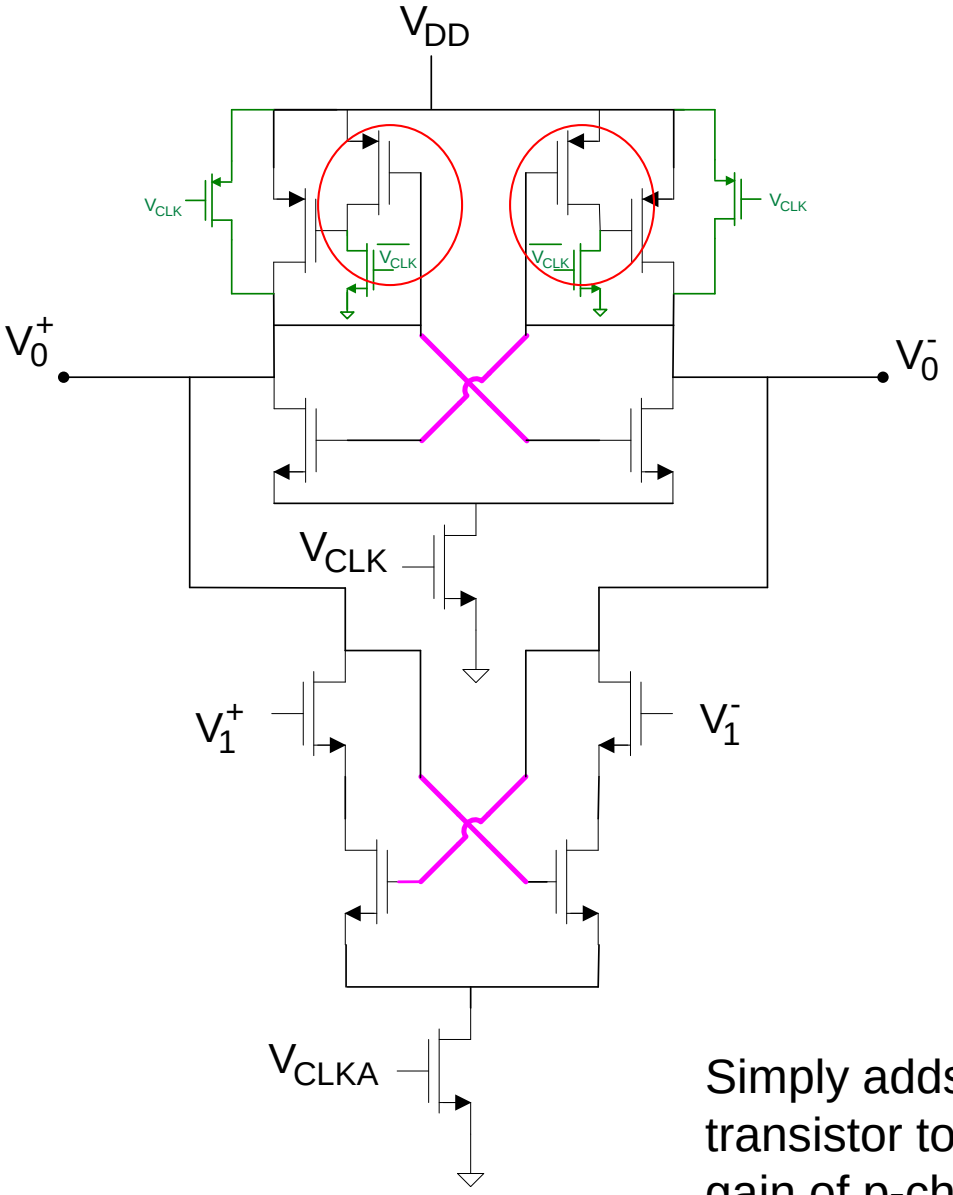


Goff ISSCC 2009 (maybe not original source)



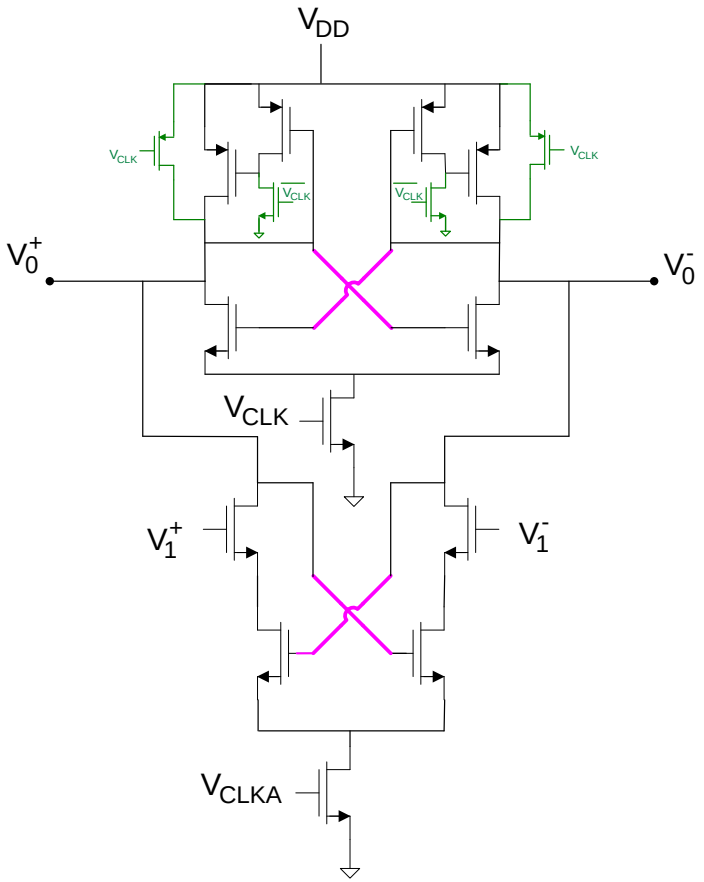
Goff ISSCC 2009

Alternate Dynamic Comparator Structure



Simply adds one more PMOS transistor to basic circuit to increase gain of p-channel load

Alternate Dynamic Comparator Structure



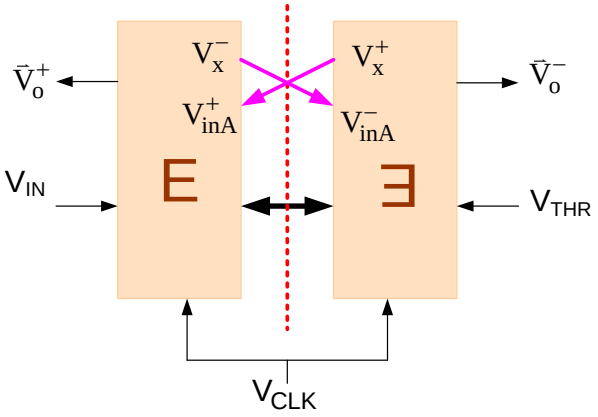
Goff ISSCC 2009

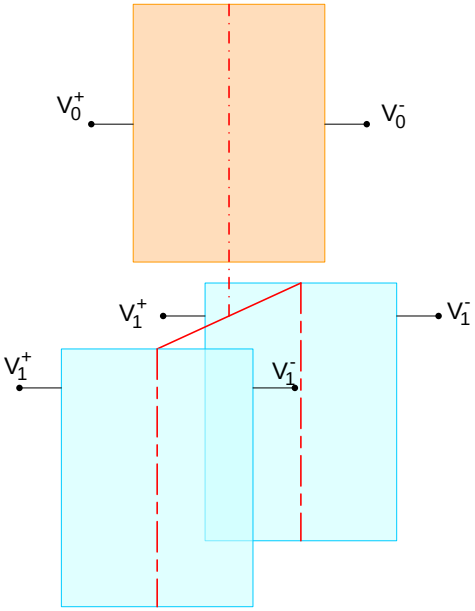
Natural questions arise -

If benefit was obtained from cascading p-channel devices in latch, how about cascading n-channel devices?

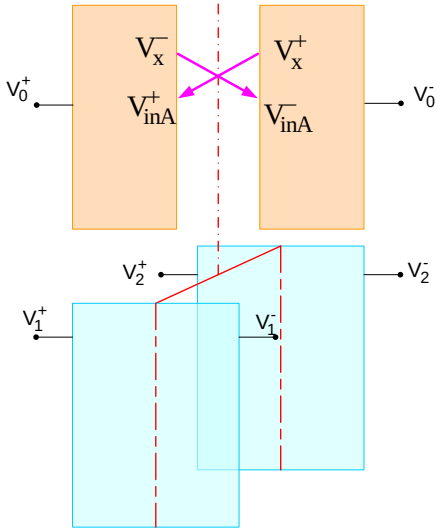
What about a fully-differential version of this concept?

Dynamic Comparator Structures





Symmetric Circuit
(V_{CLK} not shown)

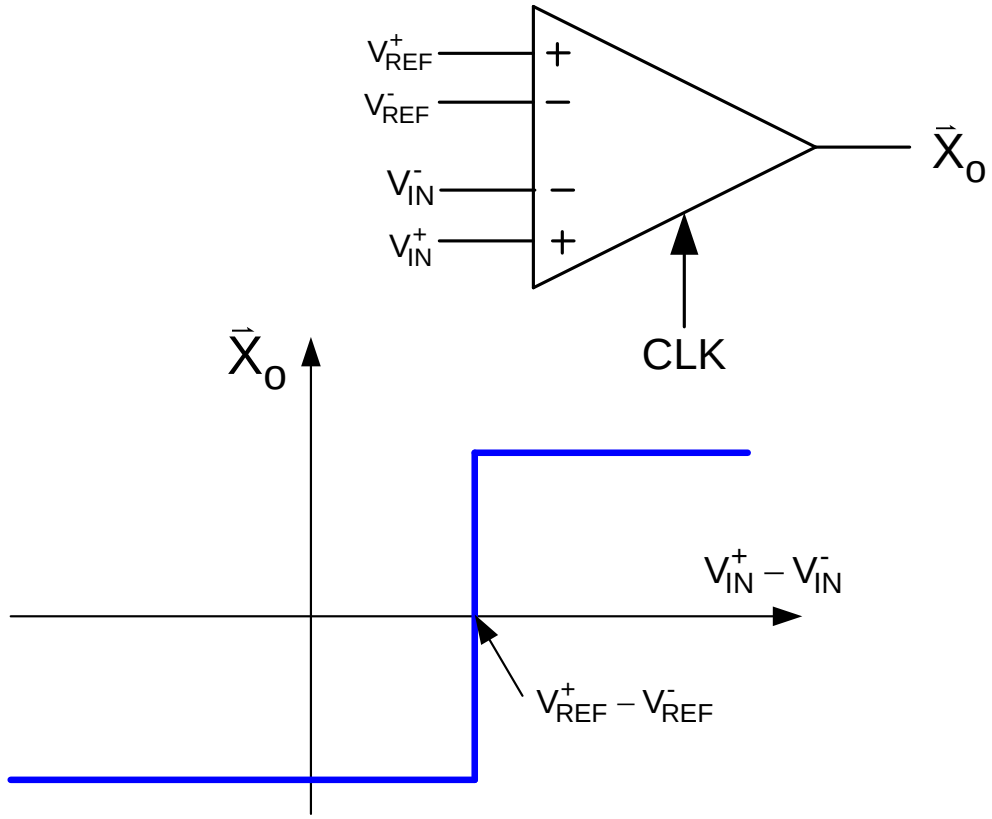


Symmetric Circuit with Regenerative Feedback (V_{CLK} not shown)

- Symmetric Circuit need not be planar
- Differential comparators often not planar

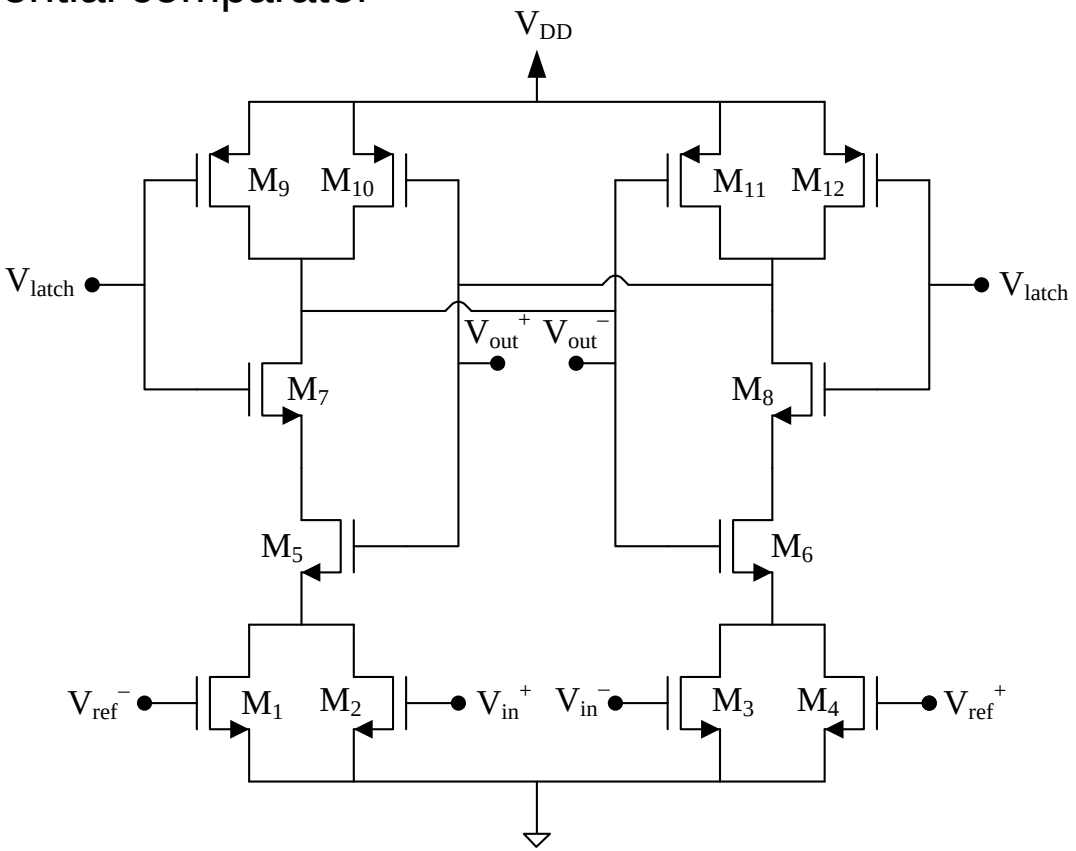
Differential Comparator

A differential comparator is a circuit that provides a high Boolean output if the differential input is positive and a low Boolean output if the differential input is negative



Differential Comparator

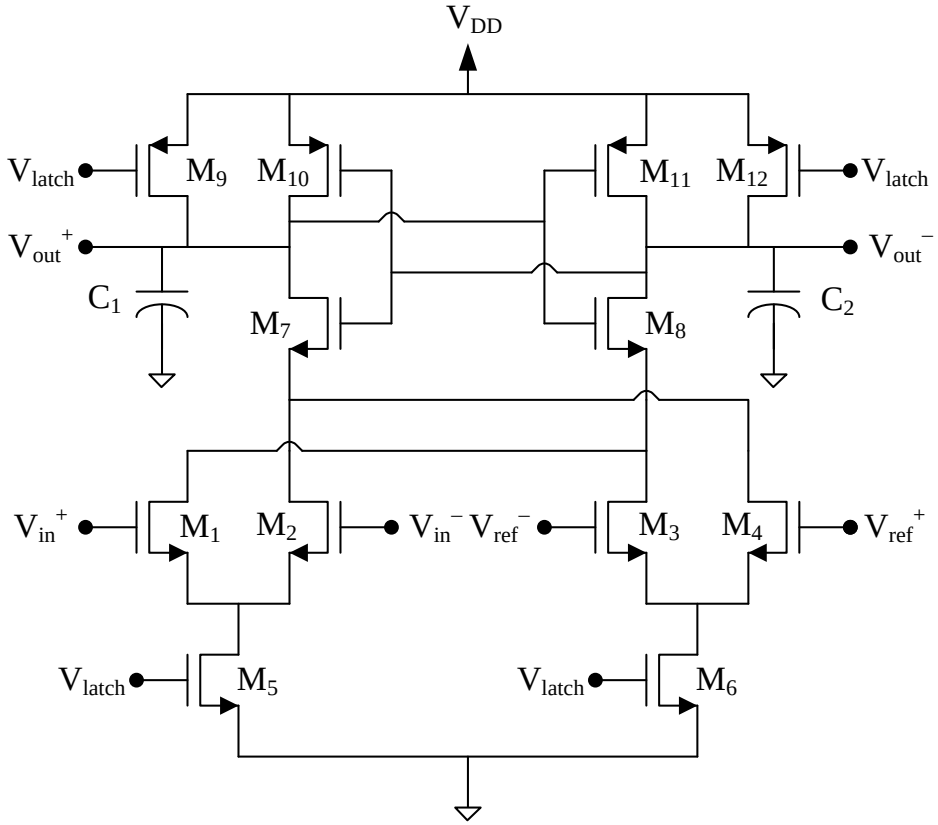
Popular differential comparator



Lewis – Gray Comparator

Differential Comparator

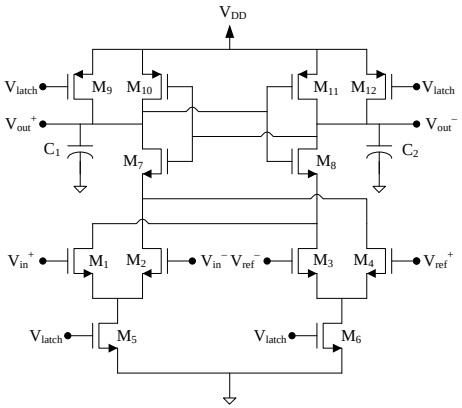
Popular differential comparator

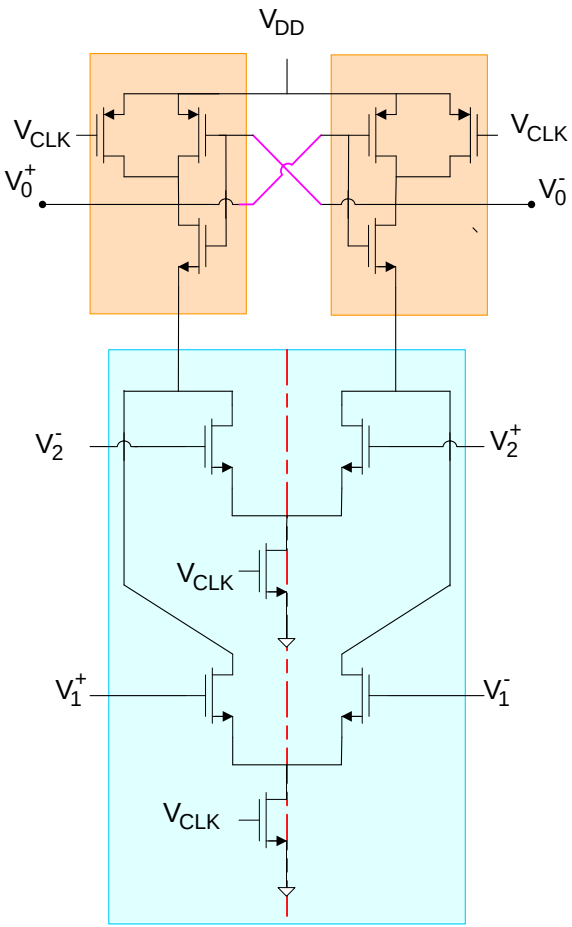


Halonen Comparator

Differential Comparator

Popular differential comparator

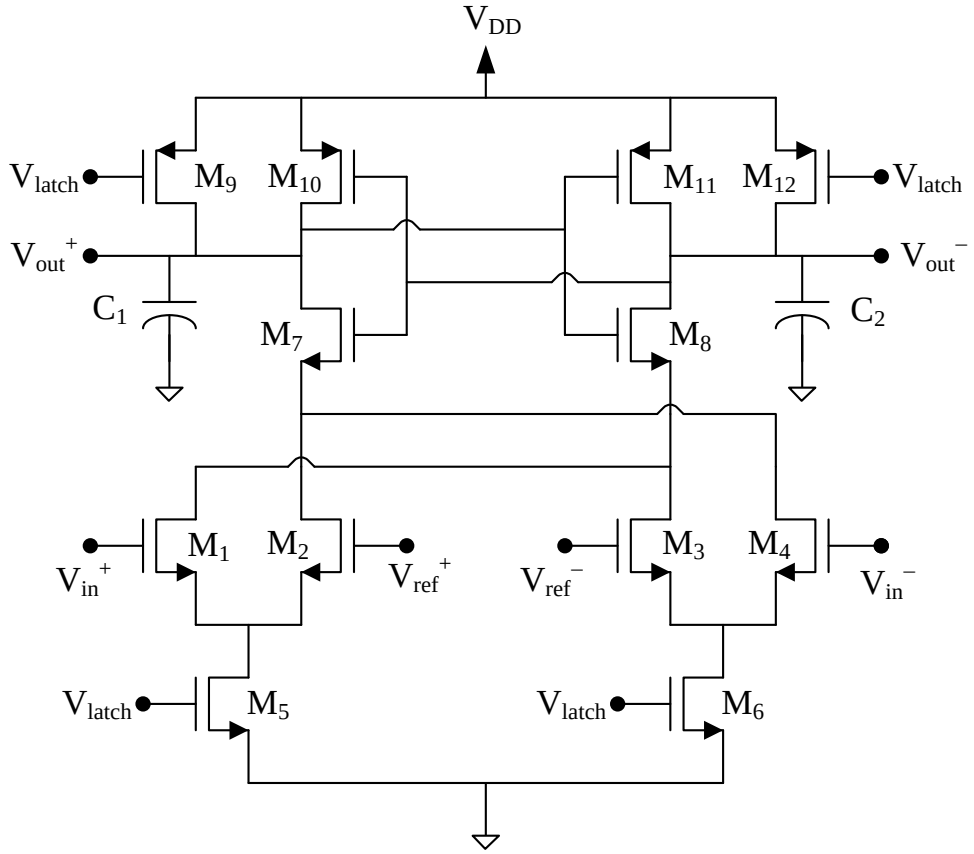




Halonen Comparator

Differential Comparator

Popular differential comparator

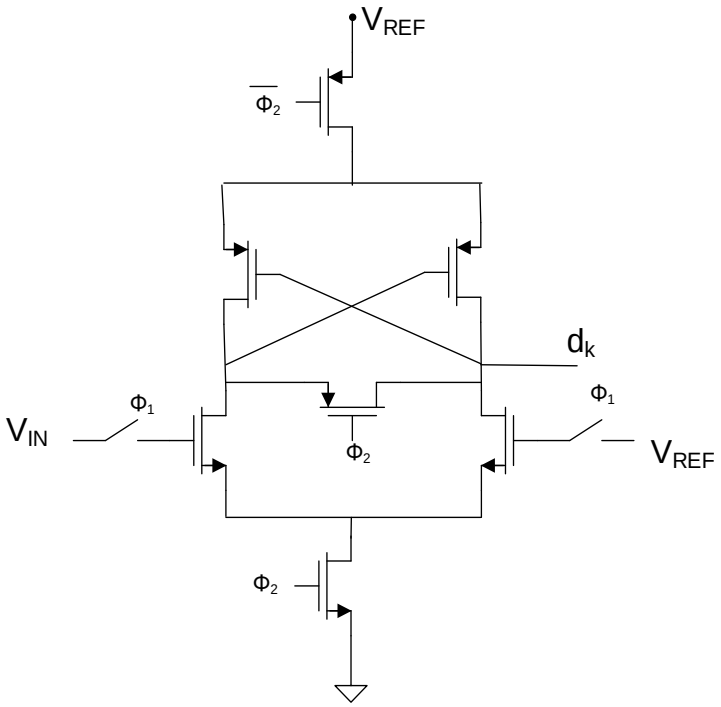


Katyal Comparator

Dynamic Comparator Opportunities

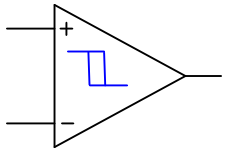
- Dynamic Comparators can easily be designed
- Likely some of best structures have not evolved
- Symmetric circuit with regenerative feedback gives opportunity to identify new structures that may be particularly useful

Clocked Comparator with Regenerative Feedback

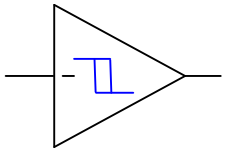


Regenerative Feedback

Regenerative Comparators



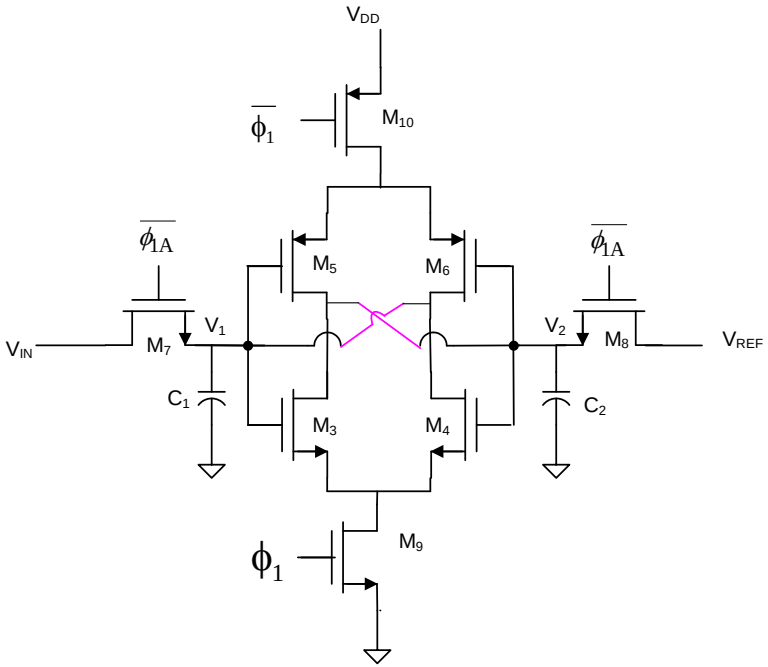
Differential

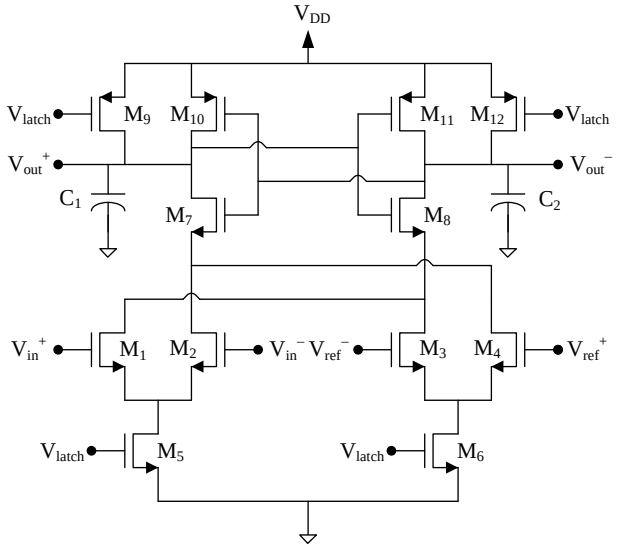


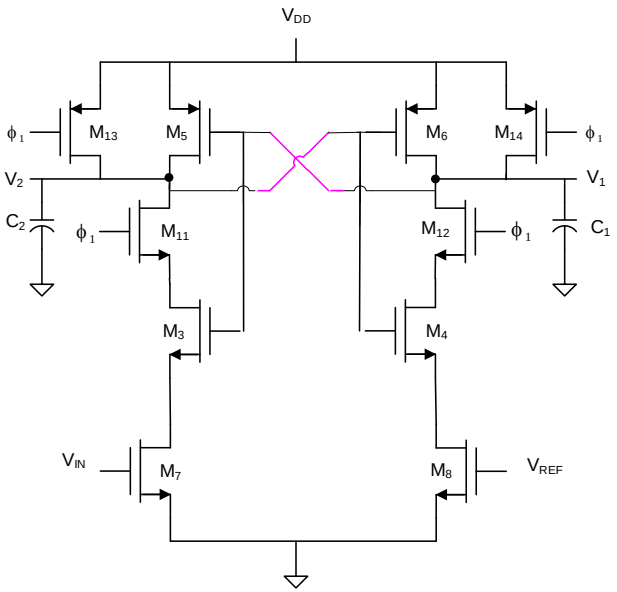
Single-Ended

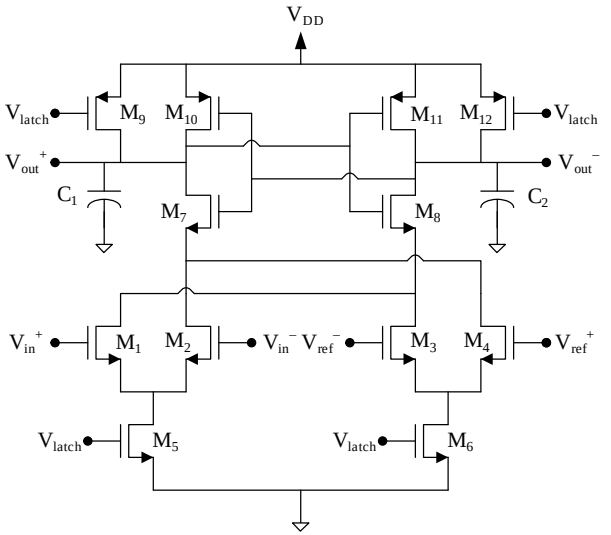
- Regenerative feedback often used to force decision when differential inputs are small
- Several variants of clocked comparators are available
- Important to not have trip point dependent upon previous comparison results
- Often one or more linear gain stages precede the regenerative stage
- Power dissipation can be small in regenerative feedback comparators
- Large offset voltage (100mV or more) common for regenerative feedback comparators

Clocked Comparator with Regenerative Feedback

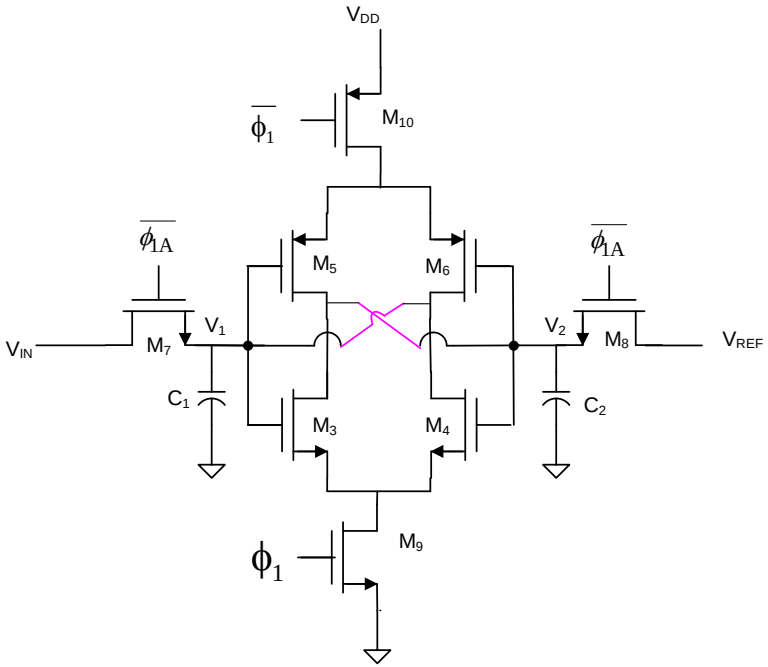








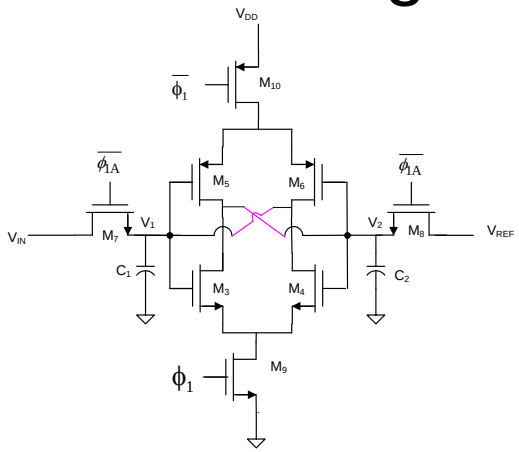
Clocked Comparator with Regenerative Feedback



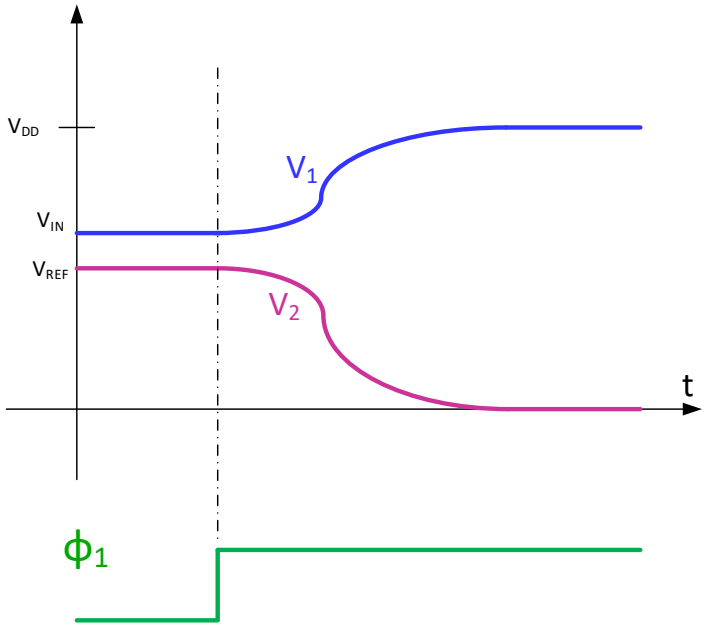
Advanced clock samples inputs on input to digital latch cell

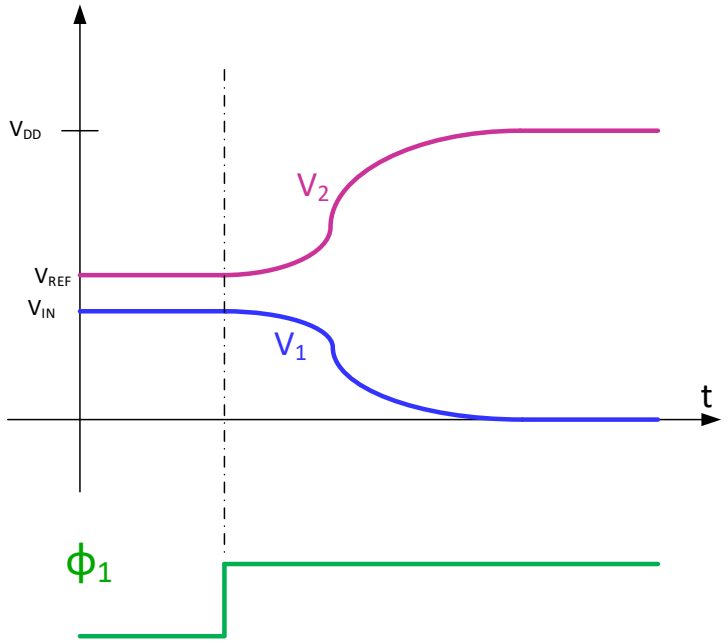
During regenerative state power dissipation goes to 0 after decision is made

Clocked Comparator with Regenerative Feedback

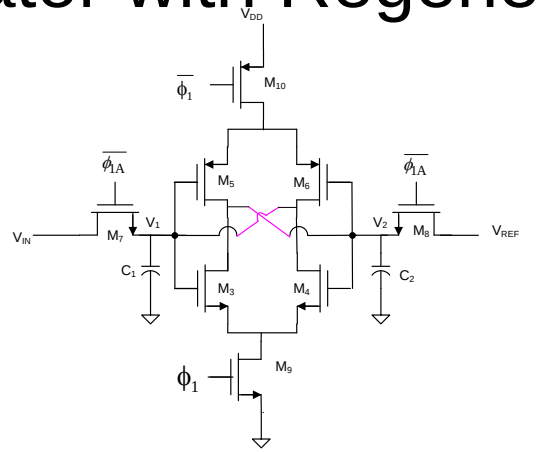


Desired Response

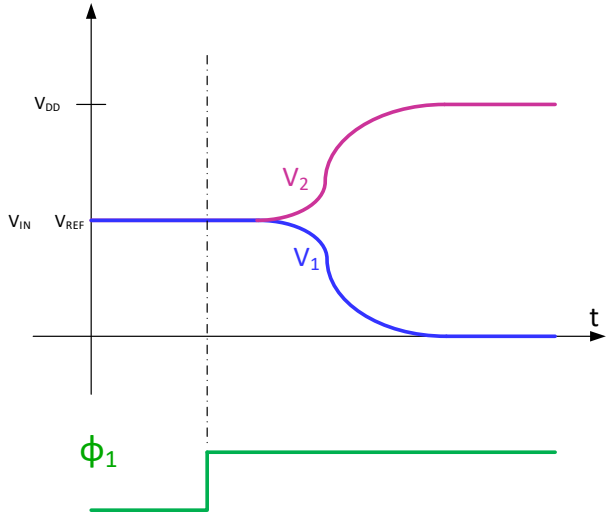


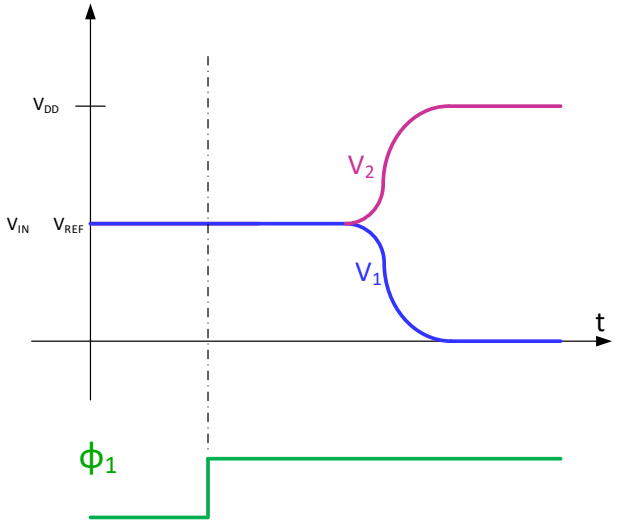


Clocked Comparator with Regenerative Feedback



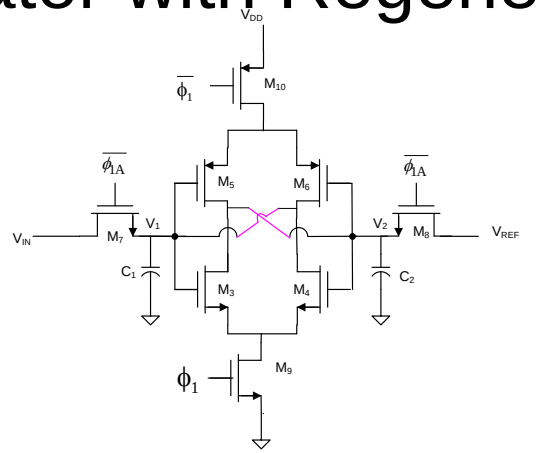
when V_{IN} and V_{REF} close to each other



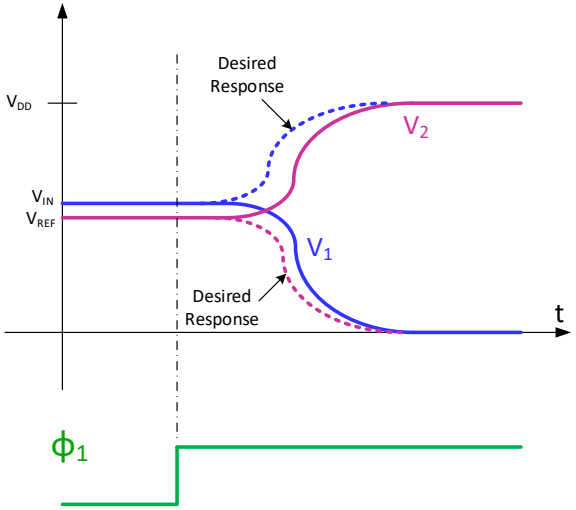


- decision delayed
- may stay in metastable state until after decision must be made
- vulnerable to making wrong decision due to offset or noise

Clocked Comparator with Regenerative Feedback

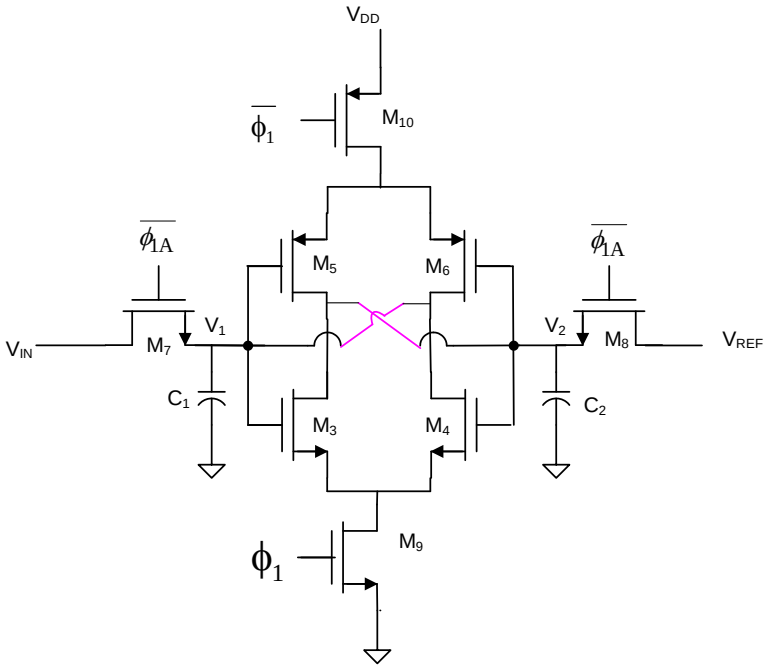


when V_{IN} and V_{REF} close to each other



- wrong decision when close (exaggerated)
- almost always only concerned about when V_{IN} close to V_{REF}

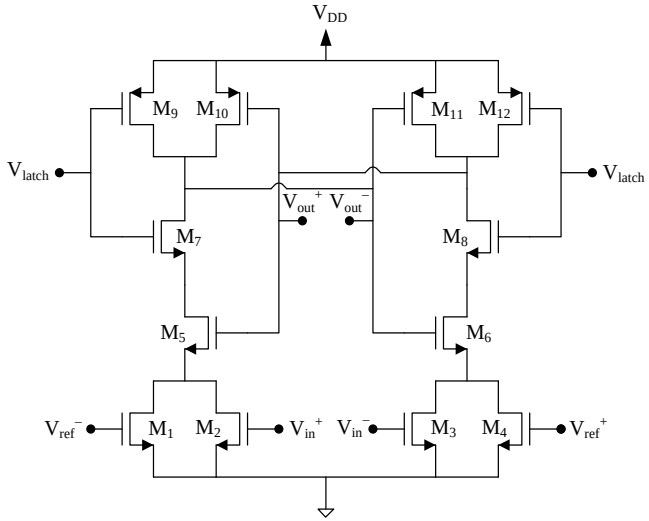
Clocked Comparator with Regenerative Feedback



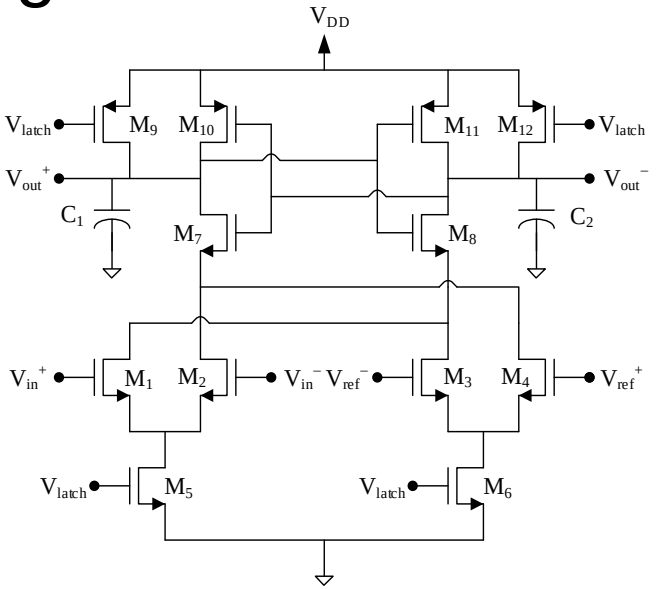
Dominant causes of offset voltage of comparator

- Missmatch of parasitic capacitance on V_1 and V_2 nodes
- Missmatch in digital inverter trip points (particularly in weak inversion)
- Missmatch on advanced clocks (timing and parasitic capacitances)
- Missmatch of charge injection of advanced clocks
- Missmatch of leakage diffusion currents
- Assymetry in layout of cross-coupled structures
- Noise when in weak inversion

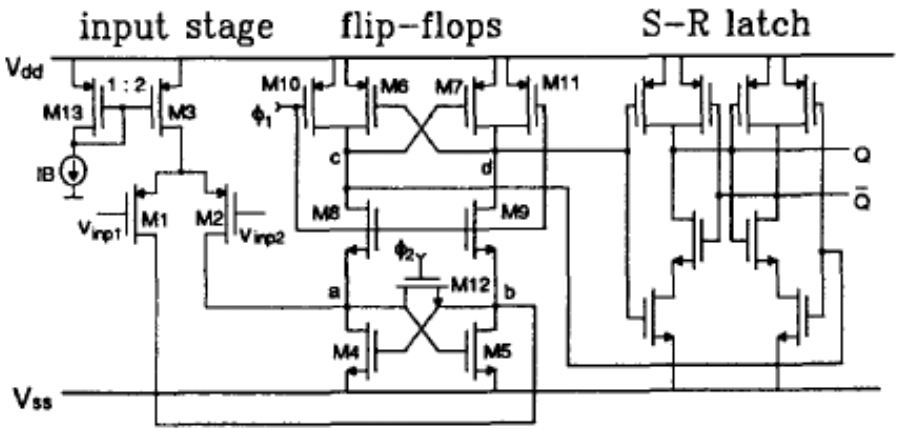
Clocked Comparator with Regenerative Feedback



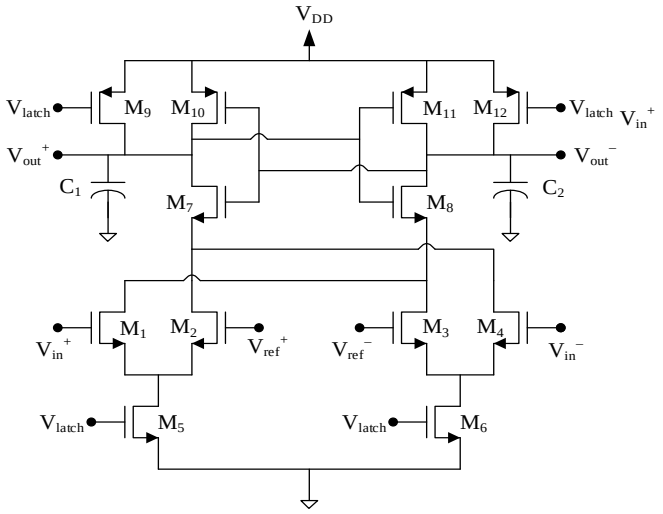
Lewis Gray Comparator



Halonen Comparator

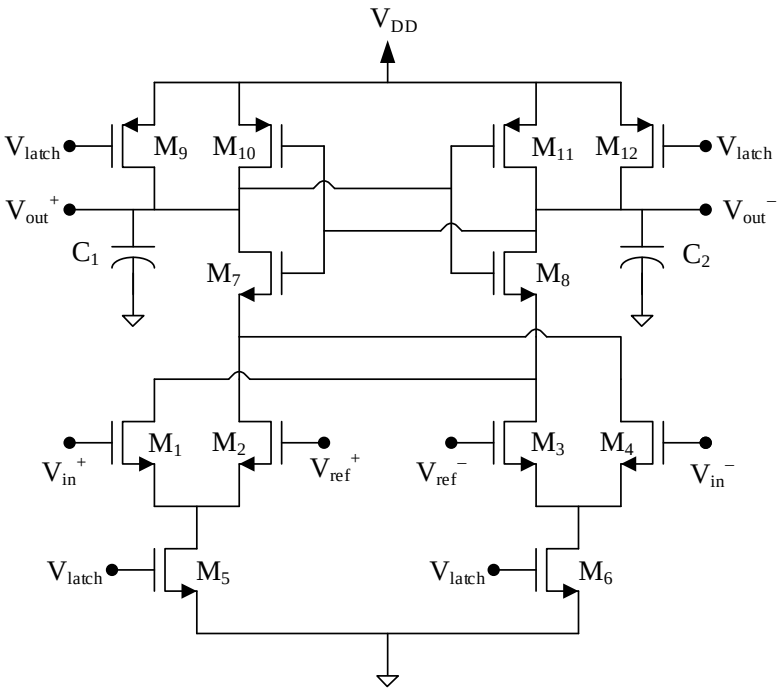


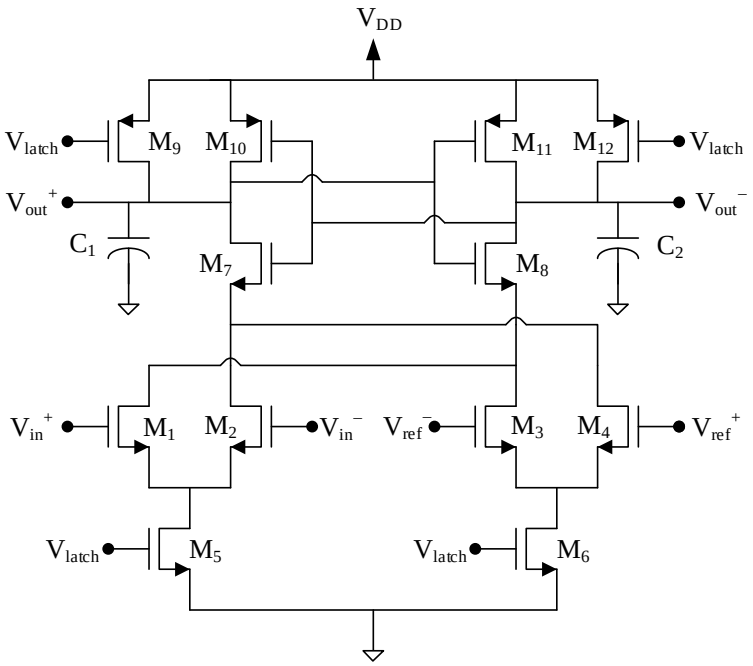
Sansen 92



Katyal Comparator

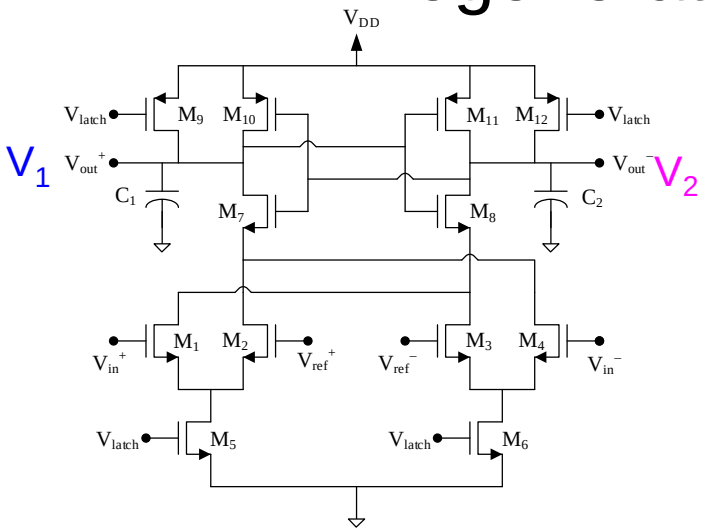
Katyal and Halonen Comparators with Regenerative Feedback

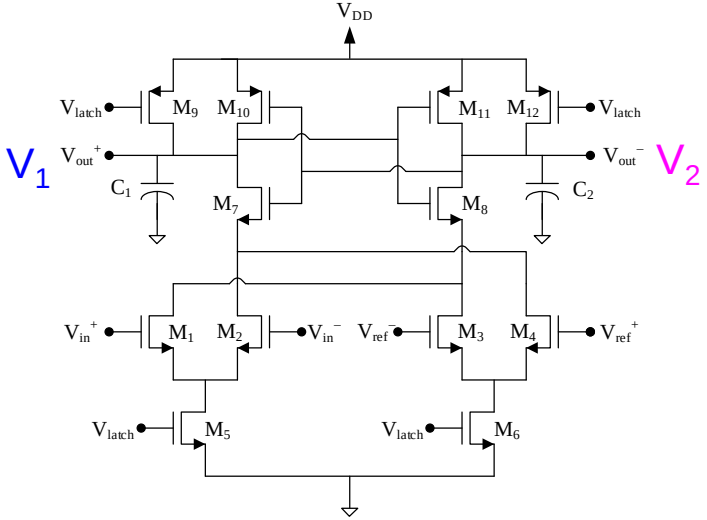




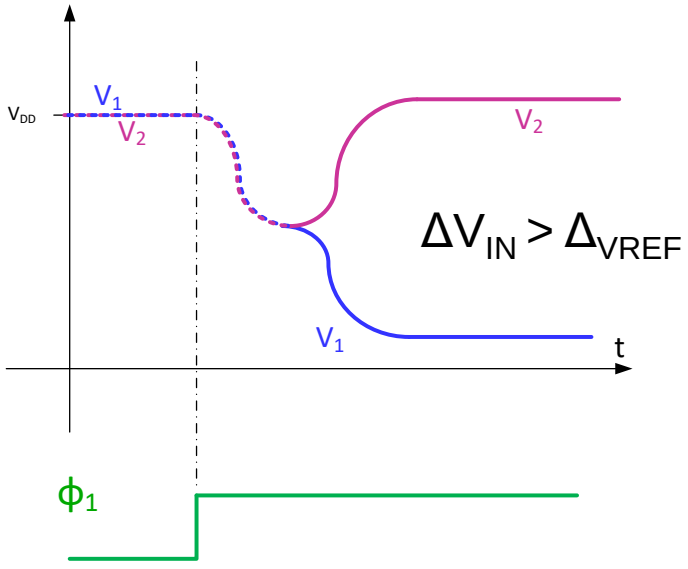
- Outputs precharge to V_{DD}
- Current is steered to left or right side depending upon input differences
- Phasing of upper latch and lower latch signal may be different
- May limit swing on latch signals (switch versus current source in tail)
- Small previous-code dependence due to residual voltages on sources of M_7 and M_8

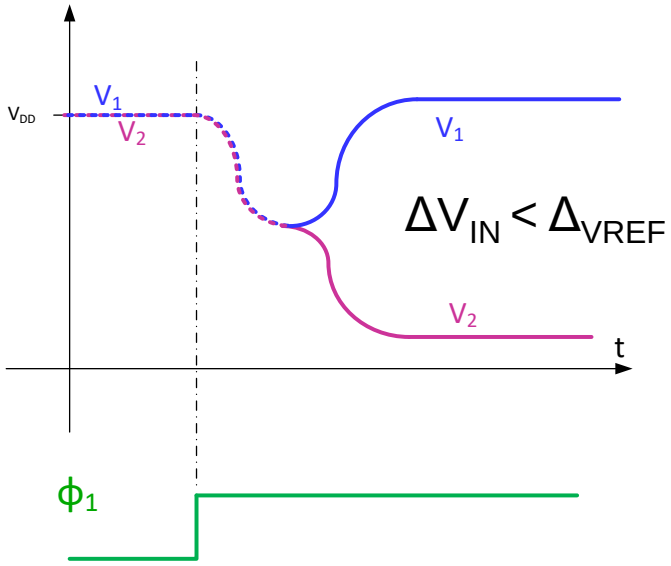
Katyal and Halonen Comparators with Regenerative Feedback



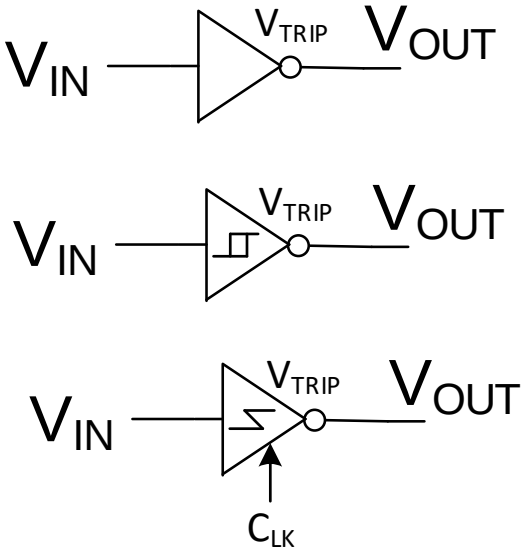


Ideal Responses



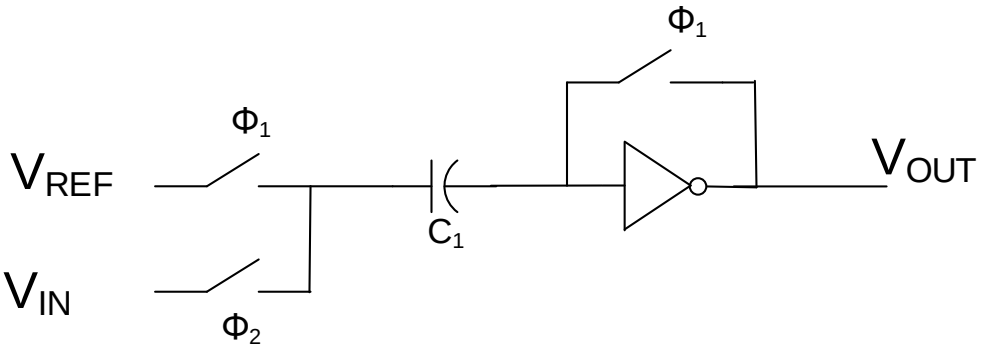


Single-Ended Comparator w/o Reference



- Reference embedded in inverter trip point
- Device dimensions can set trip point
- Could be extremely small
- Highly dependent upon process variations
- Calibration can be used to trim trip points

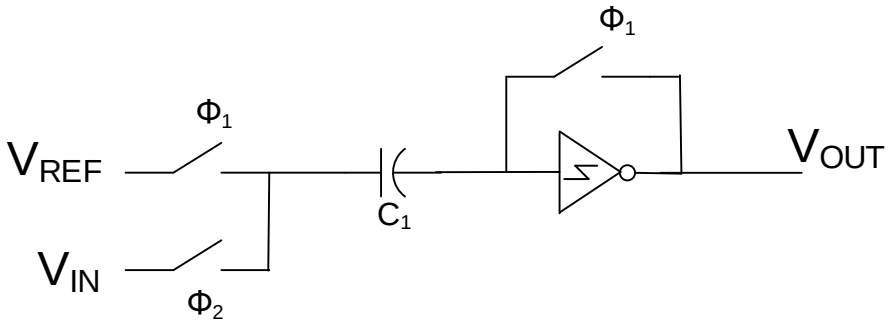
Clocked Linear Comparator with Offset Compensation



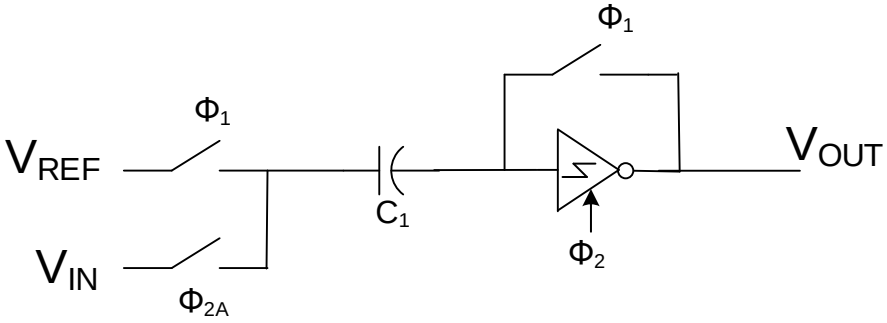
Preamplifier or Linear Comparator with offset compensation

- Ideally removes all offset effects
- May not have a large enough gain
- Offset Compensation can be added to regenerative latches
- Several variants of offset compensation circuits are available

Offset Compensation

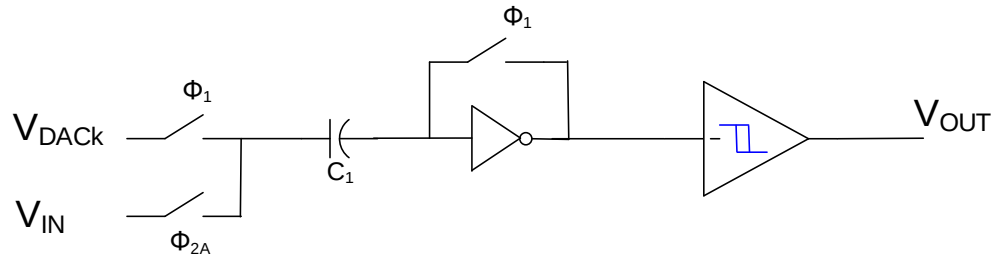


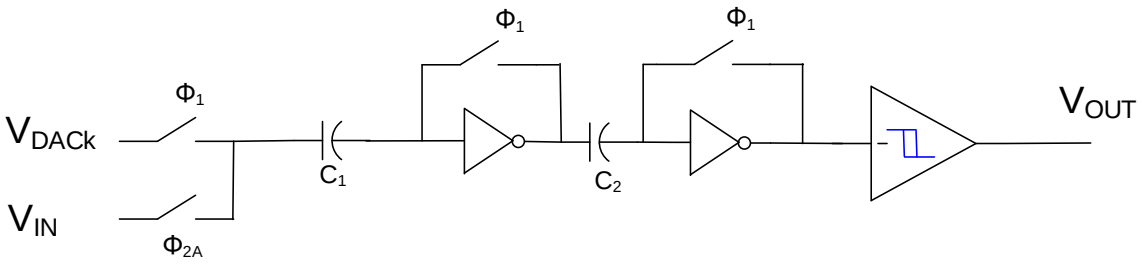
Preamplifier or Regenerative Feedback can be added to amplifier

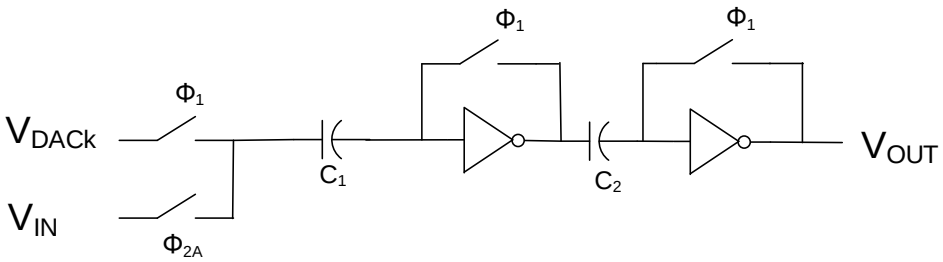


Comparator can be clocked following linear amplifier phase

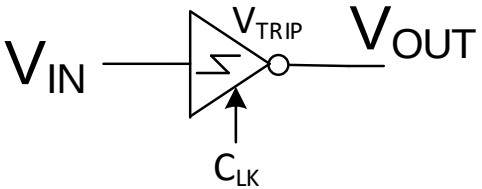
Some Variants of Clocked Offset Compensation

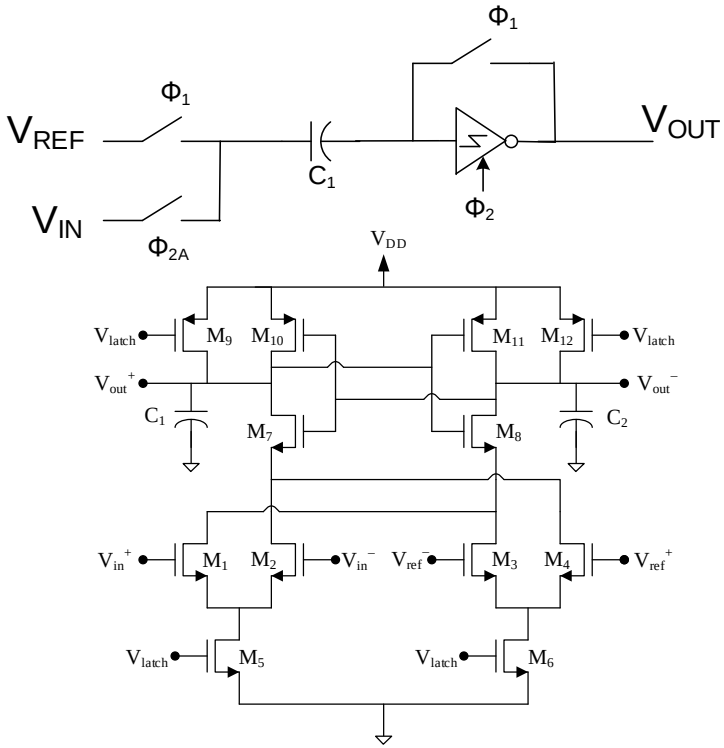


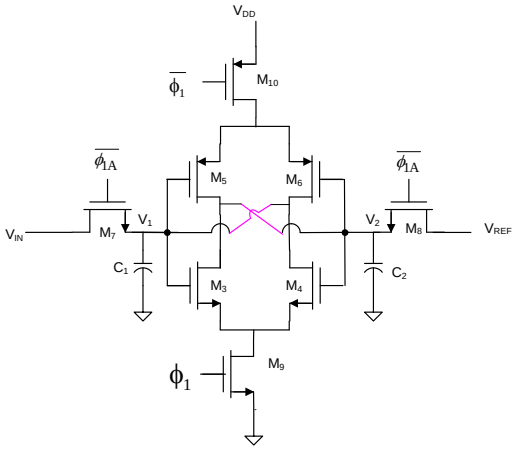




Where are poles of regenerative comparators located?







In RHP !

Is stability of concern?

No ! Want positive real axis poles (i.e. unstable circuit) to force decision

Stay Safe and Stay Healthy !

End of Lecture 19